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# Improving the light-induced degradation of hydrogenated amorphous silicon solar cells using fabrication at elevated temperatures and low pressure

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**Improving the light-induced degradation of hydrogenated amorphous silicon solar cells using fabrication at elevated temperatures and low pressure**

by

**Brian Joseph Modtland**

A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:  
Vikram Dalal, Major Professor  
Rana Biswas  
Mani Mina

Iowa State University  
Ames, Iowa  
2013

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## ABSTRACT

A method of fabricating hydrogenated amorphous silicon (a-Si:H) solar cells that reduces light-induced degradation via the Staebler-Wronski effect is presented. By using elevated temperatures up to 450°C with chamber pressures down to 25mT, a-Si:H solar cells are fabricated with improved stability. This combination of fabrication conditions, combined with a gradient of boron doping (ppm) in the intrinsic layer creates solar cells with a measured degradation of only 10% compared to almost 25% for standard devices. Defect density measurements before and after light exposure confirm that midgap trap states are not changed as much as in standard devices. This indicates less light-induced defects are created which ultimately reduce solar cell efficiency.

All samples were fabricated and measured at the Microelectronics Research Center at Iowa State University. Devices were made using a single chamber plasma-enhanced chemical vapor deposition (PECVD) reactor operating at 45MHz. Standard measurements included current versus voltage, external quantum efficiency, capacitance spectroscopy, and subgap quantum efficiency.

Light degradation testing was performed using a custom setup that was designed and built at the MRC. The light soaking apparatus allows for automated, in-situ measurements of samples while being exposed to simulated sunlight (AM1.5) for variable amounts of time and intensity.

The method of fabrication that is ultimately presented was arrived upon after systematically studying devices with other fabrication parameters. These results are also given to show the logical progression of attempts and the eventual outcome.

## CHAPTER 1 - INTRODUCTION

Thin-film photovoltaics have become a low-cost solution to electricity generation from sunlight. Of the available options, amorphous silicon (a-Si) has been studied for many decades because of its many advantageous properties over traditional crystalline silicon (c-Si). In particular, amorphous silicon as a material can absorb light more effectively than its crystalline brethren due to the larger number of allowed optical transitions as a result of the disordered structure. Unfortunately, this disorder also reduces charge transport, making photo-generated electron-hole pairs difficult to collect as current. Overall amorphous silicon is at a disadvantage and devices have a lower fill factor and current density.

The main advantage of using amorphous silicon as a photovoltaic material is due to its ease of fabrication. Using chemical vapor deposition, large area cells and modules can be made commercially in a roll-to-roll process or similar. Thus, amorphous silicon solar cells are found in low cost applications regardless of the limited efficiency.

Amorphous silicon is also easy to deposit on a multitude of substrates because of its low fabrication temperature [1]. Possible substrates include glass, plastics, and various metal sheets. Of these substrates, some are thin, cheap, and flexible. This opens the opportunity for a-Si cells to be made for flexible applications, like portable chargers for consumer electronics or shingles for building integration. With physical flexibility comes flexibility in applications.

Besides poor transport properties, the main disadvantage of amorphous silicon is the degradation of efficiency that occurs when exposed to sunlight. While this immediately seems to contradict the purpose of the device, the degradation eventually saturates at manageable efficiency levels. Table 1-1 provides a summary of the main advantages and

disadvantages of using amorphous silicon over crystalline silicon when making photovoltaic cells.

**Table 1-1. Advantages and disadvantages of a-Si used in PV compared to c-Si.**

Advantages	Disadvantages
<ul style="list-style-type: none"> <li>• Better absorption coefficient (larger <math>\alpha</math>)               <ul style="list-style-type: none"> <li>• Larger voltage (Larger <math>E_g</math>)</li> <li>• Flexible/cheap substrates</li> </ul> </li> <li>• Easier fabrication with CVD               <ul style="list-style-type: none"> <li>• Roll-to-roll processing</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>• Low mobility</li> <li>• Low recombination times (ns)</li> <li>• Only absorbs below 700nm well (<math>E_g \sim 1.8\text{eV}</math>)               <ul style="list-style-type: none"> <li>• Light-induced degradation</li> <li>• Lower efficiencies</li> </ul> </li> </ul>

While the solid-state properties of a-Si prevent high carrier mobility and long diffusion lengths, device structure and fabrication can be altered to improve light-induced degradation so that stabilized efficiencies are competitive with other technologies. In this research, work is presented that improves the light-induced instability that occurs in solar cells made from hydrogenated amorphous silicon.

## 1.1 Motivation for Thin-film Solar Cells

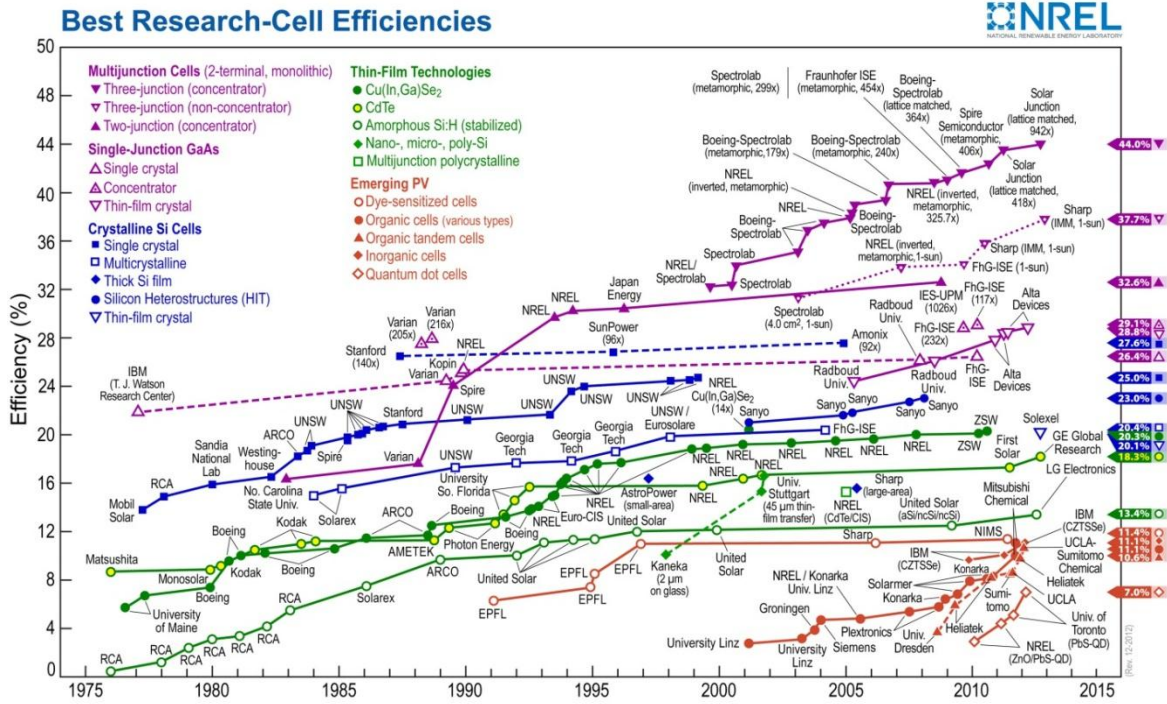
By 2050 the human population is expected to balloon to nearly 10 billion [2]. The projection is that civilization will consume around 30TW of power at that time [3]. With declining supplies of fossil fuels and concern for global climate change due to the emissions from combustion of hydrocarbons, there exists a large gap to be filled by other sources of electricity. One of the least utilized sources is energy from the sun. Whether from passive heat, solar thermal, or photovoltaic, a large reservoir of energy is present for humanity to harvest. The solar power that passes to the surface of the planet is around 89PW, meaning only 0.034% of this power needs to be harvested to provide all of our power in the future [4]. Although not realistic, the potential that exists is obviously large and will not disappear without apocalyptic consequences.

Unfortunately, the current methods of converting the sun's energy to usable forms are quite inefficient and require a lot of land at a hefty cost. In 2013, the cost of electrical energy from PV is still around \$5/Watt when considering all of the components and infrastructure required in addition to the solar modules [5]. At this point in time, the cost of modules is near \$1/W with the other \$4/W coming from inverters and the physical structure required for mounting. Even lowering the cost of each module will not remove these costs unless efficiencies are increased. To truly reduce the cost of photovoltaic electricity the power conversion efficiencies of cells needs to be improved. This reduces the area required for a given amount of power, drastically lowering cost more so than lowering the cost of the cells alone.

The goal then is to improve efficiencies in current technology while not sacrificing cost of production to decrease the total cost per watt of photovoltaic energy. In addition, there are many applications which could benefit from solar power but rigid PV is not a solution. For example, military units carry many batteries for all of their electronics. A lightweight, portable solar panel which folds would be an ideal solution. For these applications, thin-film solar cells are ideal. These niche applications require less infrastructure cost but still require the largest possible efficiencies to reduce cell area for reasonable power output.

Figure 1-1 shows a plot of the NREL confirmed record efficiencies for PV cells using different technologies [6]. Thin-film cells are given in green with the stabilized a-Si:H efficiency having a recently reported record of 13.4% by LG Electronics [7]. Compared to c-Si and the III-V concentrator cells, this efficiency is meager meaning utility sized usage is not realistic. Fortunately, compared to the other flexible technologies, a-Si:H has one of the

largest record efficiencies. Other thin-film technologies such as organic PV and quantum dots are far behind but fast approaching as research continues.



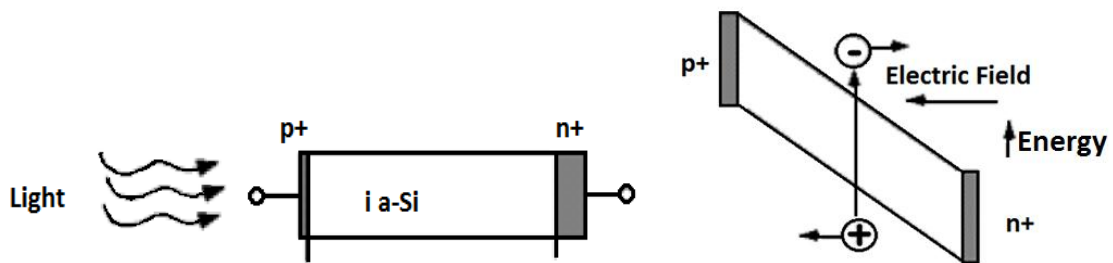
**Figure 1-1. Graph of record efficiencies for each PV technology over time as reported by the National Renewable Energy Lab [6].**

For the most part, the efficiencies of a-Si:H solar cells are near their limit. According to detailed balance calculations by Shockley and Queisser in 1961 for a sun at 6000K, the maximum efficiency of a single-junction solar cell is 44% using a band gap of 2.2eV [8]. Further calculations using the AM1.5 solar spectrum show this maximum to be closer to 33% using a material with a bandgap of 1.4eV [9]. For a-Si, the band gap is ~1.8eV giving a theoretical thermodynamic efficiency of ~22% [10]. Since a-Si is not an ideal crystal with  $E_g=1.8\text{eV}$  there are many non-idealities that reduce this efficiency. In addition, these theoretical maximums do not account for degradation. Thus, to improve efficiencies in a-Si:H devices, the light-induced degradation needs to be improved without compromising initial efficiency or manufacturability.

## 1.2 Physics of Amorphous Silicon Thin-Film Solar Cells

Typically a-Si:H cells are made from a PIN structure instead of the PN junction common for crystalline silicon cells. This is a consequence of poor carrier transport, requiring drift to assist with carrier collection. Although similar to a PN junction, the physics of a PIN junction is different based on transport aided by a built-in electric field provided by the separation of quasi-Fermi levels in the heavily doped regions. In addition, carrier transport in a-Si is controlled by midgap defects which act as recombination centers.

Figure 1-2 shows the physical structure and energy band diagram of a PIN diode. Normally, the separation between quasi-Fermi levels in the p+ and n+ regions creates a built-in electric field which generates a depletion region at the junction. In a PIN device the transition between p+ and n+ regions takes place uniformly throughout the intrinsic layer. Thus, the built-in electric field in thermodynamic equilibrium is roughly linear in the i-layer allowing any photo-generated carriers to be swept to their respective contacts for collection. Increasing bias decreases the strength of the field while negative bias augments it. This is simplified by stating that PIN solar cells depend on drift of carriers whereas PN cells primarily operate based on diffusion.

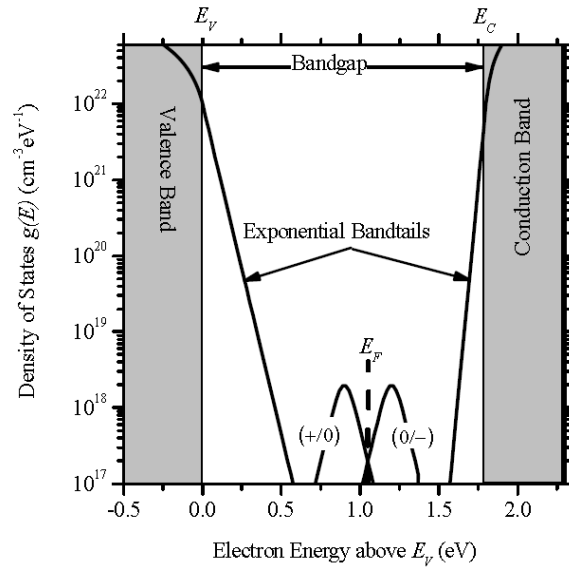


**Figure 1-2. Energy band diagram for a PIN junction.**

Since amorphous silicon has no long range atomic order, the density of states image typical of crystalline semiconductors is altered. In amorphous silicon, each silicon atom has

the potential to bond to four neighbors. Unlike with crystalline silicon, these bonds are not uniform. Bond lengths and angles are different than the diamond structure changing the band diagram. This leads to tail states that exponentially decay away from the band edges (see Figure 1-3). Absorption measurements confirm these states are exponential and can be used to indicate film quality (see Chapter 3).

The other defects that are present in a-Si are the deep midgap states caused by film defects. One of the most common causes of these states is missing valence bonds, commonly called “dangling” bonds. The next section explores how these defects relate to light-induced degradation. These defects also act as strong trap states, reducing minority lifetime and limiting the ability for carriers to be collected. Since diffusion lengths are low with high recombination, the i-layer must be made thin ( $\sim 0.3\mu\text{m}$ ). Fortunately, absorption in a-Si is strong providing enough carriers for current densities above  $10\text{mA}/\text{cm}^2$ .



**Figure 1-3. Density of States diagram typical of a-Si:H. Notice the exponential band tail states near the band edges plus the deep midgap states with different charge states [11].**

As mentioned before, a strong built-in electric field allows carriers to be collected by a solar cell. In addition, two other parameters are indicative of a good device with sufficient

carrier transport and collection. The first is mobility. In a-Si:H common values for mobility are in the range of  $10 \text{ cm}^2/\text{V}\cdot\text{s}$  which is at least one order of magnitude lower than most semiconductors [12]. This low mobility is mostly due to the material's disorder which makes scattering more prevalent as free carriers try to move through the lattice.

The second important parameter is minority carrier lifetime  $\tau$ . Since amorphous silicon contains many deep trap states, the recombination time is determined by Shockley-Read-Hall (SRH) trap-controlled recombination. Based on recombination-generation statistics and detailed balance, the lifetime of carriers can be found. Equation 1-1 gives the formula for hole lifetime given a single trap level with a capture cross section of  $C_p$  and a trap density of  $N_T$ . This gives an approximate description that lifetime will decline as the number of traps increase. Since a-Si contains a continuous profile of midgap defects a more exact expression can be obtained from Simmons and Taylor [13].

$$\tau_p = \frac{1}{C_p N_T} \quad (3-1)$$

Combined, the product of mobility and minority recombination time is used to indicate carrier transport in a-Si. For devices with the same built-in field, the device with the largest  $\mu\tau$  product will have the highest collection of EHPs. In intrinsic amorphous silicon the  $\mu\tau$  product for holes is much less than for electrons. Typically,  $\mu\tau$  is around  $10^{-8} \text{ cm}^2/\text{V}$  for holes and  $10^{-6} \text{ cm}^2/\text{V}$  for electrons [1]. This means that holes are effectively the minority carriers and are of most concern in photovoltaic devices. Henceforth, measurements and discussion of carrier collection are primarily concerned with holes since they are the minority carriers in the intrinsic layer.

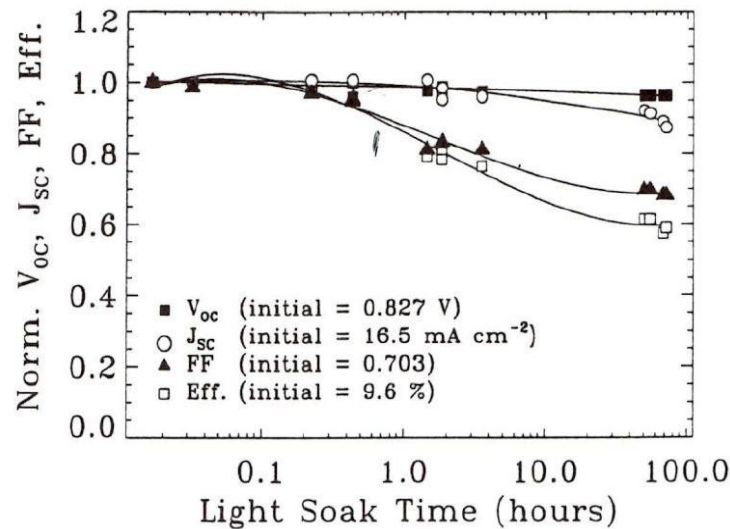
Assuming  $\mu\tau_p = 10^{-8} \text{ cm}^2/\text{V}$  and the i-layer thickness is  $0.3 \mu\text{m}$ . In order to collect holes with high efficiency, the built-in electric field must be  $3000 \text{ V/cm}$  or  $0.09 \text{ V}$  over that layer.



This is manageable with a band gap of 1.8eV. Under forward bias and after degradation the built-in field is reduced, but the goal is to keep the drift large enough to collect all carriers.

### 1.3 Light-Induced Degradation in a-Si:H Solar Cells

In 1977, Staebler and Wronski discovered that films made from amorphous silicon degrade in quality when exposed to sunlight [14]. Used in solar cells, this light-induced degradation, also known as the Staebler-Wronski effect, results in a loss of efficiency over time. Figure 1-4 shows a typical result of degradation with light exposure that was observed by Von der Linden in 1994 [15]. Over 100 hours of exposure to 100mW/cm<sup>2</sup> light (one times sunlight intensity) caused cell efficiency to drop by 40%. This decline was mostly due to a drop in fill factor with only a slight degradation in  $V_{OC}$  and  $J_{SC}$ .



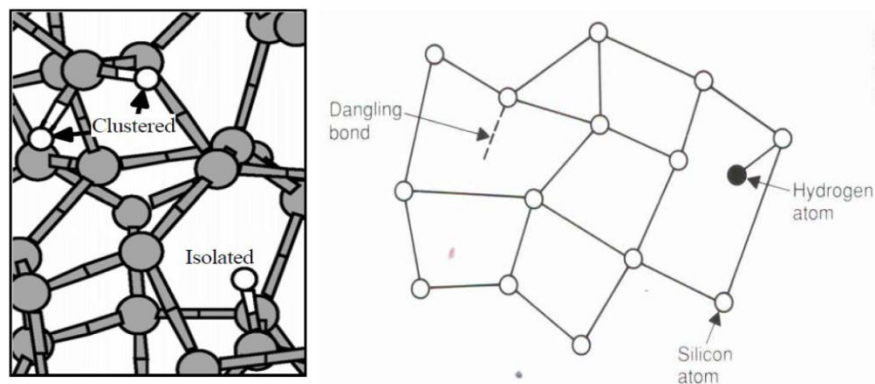
**Figure 1-4. Changes in I-V values as an a-Si:H cell is exposed to AM1.5 light at 100mW/cm<sup>2</sup> [14].**

While the proposed mechanism for degradation is still evolving with time, the accepted consensus is that it has to do with metastable defects in the material. When amorphous silicon is deposited on a substrate, the individual atoms of silicon must find a place on the existing layer. Bonding which reduces the potential energy of the atom the most

is preferred just as  $H_2$  is preferred over  $2H$ . Since energy applied to the system during fabrication is low, the layer that forms is not a perfect crystal but is disordered. An order between atoms may exist over nanometers of space, but the material is generally considered disordered especially when compared to polycrystalline films.

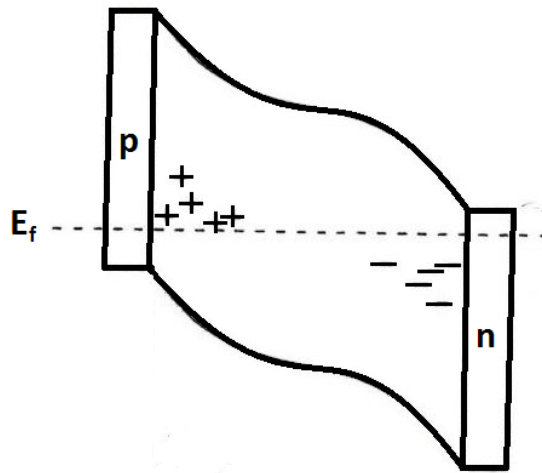
Disorder means that bond angles and lengths are different in all directions between all bonding atoms. Occasionally a silicon atom sits where it only shares three valence electrons instead of the four which it can support. The final valence electron acts as a defect state which prefers holes for recombination. Because this defect is localized around an atom with one less covalent bond than expected, it is often called a “dangling bond”.

To fix the problem created by dangling bonds, that being excess recombination centers, hydrogen gas can be used in addition to silane during deposition. In the correct ratios, this hydrogen works to fill these bonds as in Figure 1-5. Device quality a-Si:H has 5-10% hydrogen in the lattice [9]. Unfortunately, high energy photons in the UV and blue range can break these newly created Si-H bonds. Thus, exposure to light containing high energy radiation is expected to result in more dangling bond defects which results in a declining fill factor that reduces efficiency.



**Figure 1-5. Defect states in a-Si:H due to dangling bonds created when Si atoms only bond to three neighboring atoms instead of four. With exposure to light, high energy photons can create these defects and degrade solar cell performance [11].**

Looking at the energy band diagram of a PIN solar cell, degradation can be shown in another manner. Light exposure creates positively charged defects near the p-i interface and negatively charged defects near the n-i interface as shown in Figure 1-6. These defects distort the built-in electric field in the intrinsic layer by causing the field to concentrate in the newly created space charge regions. Since the built-in field is still the same in magnitude, the consequence is a smaller field in the middle of the intrinsic layer. Due to this light-induced band bending, photo-generated carriers in the i-layer have a lower chance of being collected, thus reducing quantum efficiency and fill factor.



**Figure 1-6. Energy band diagram for PIN solar cell with light-induced degradation that creates a weakening of the built-in electric field in the intrinsic layer, reducing collection and thereby fill factor.**

To reduce Staebler-Wronski degradation the obvious solution is to remove high energy light from the spectrum. While that is possible with UV filters this solution removes much of the spectrum that contributes to current. At 400nm, about 40% of the incident photons are collected as current. Another solution is to use tandem cells where both junctions are made from a-Si:H. The top cell is thin and acts as a filter of high energy light while not degrading due to large drift. This method is commonly implemented in commercial a-Si:H solar cells as a workaround for the degradation problem.

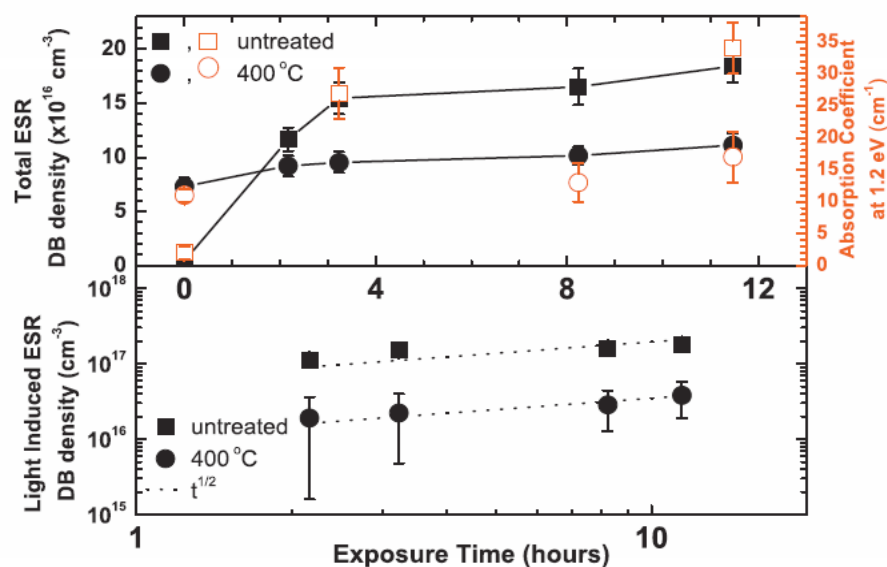
To improve light-induced degradation in single-junction cells, the main task is to improve the quality of the a-Si film in order to reduce the number of defects that exist. To reduce voids and dangling bonds during growth, the Si network needs to have little hydrogen bonding at the surface. This can be done in many ways. The goal is to keep manufacturing costs down while not sacrificing throughput in production too greatly.

A common method is to reduce the intrinsic layer thickness while keeping current density the same by using light confinement techniques. Using photonic structures and a back reflector in unison, the current density can be kept roughly equal while reducing the i-layer thickness. These photonic structures are common in thin-film PV. Unfortunately, these structures add cost and are supposed to improve current density. In this manner, a-Si solar cells have improved stabilized efficiency but not initial efficiency.

One process was proposed by Wang and Dalal that uses chemical annealing of the intrinsic layer with helium ions during growth [16]. Devices were grown layer-by-layer with periods of annealing with helium in between. During the annealing periods, helium ions bombarded the film, reducing surface defects resulting in a film with less voids. When exposed to light of  $200\text{mW/cm}^2$ , the chemically annealed samples showed less degradation. The proposed reason is a reduction in the more harmful  $\text{SiH}_2$  bonds versus  $\text{SiH}$  bonds which are more easily broken by high energy photons leading to recombination centers. While effective, this method increases the time to make a device substantially which would reduce the throughput of fabrication in a commercial setting. Similar methods of reducing dangling bond densities without hindering fabrication time are desired.

Fortunately, a recent technique of reducing dangling bond in a-Si:H films was presented by Stradins' group at NREL [17]. The group showed that annealing a-Si:H films at

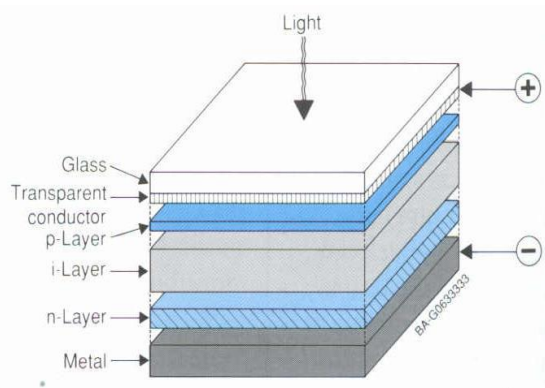
high temperatures up to 400°C for 20 minutes reduced the number of dangling bonds in the film over time when exposed to sunlight. Initially, dangling bond density was larger in the annealed film but after light exposure of a few hours the annealed films degrade less and have less dangling bonds than the untreated sample. The results of this paper are presented in Figure 1-7.



**Figure 1-7. Dangling bond density versus light exposure in films annealed at 400°C compared to untreated films. Over time, the annealed films have fewer defects than those left untreated [17].**

## CHAPTER 2 - FABRICATION OF A-SI:H SOLAR CELLS

Samples used in this study were fabricated on stainless steel substrates and consist of a PIN diode stack topped by a transparent anode. The layer stack of the devices is given in Figure 2-1. The samples that were studied by light soaking had a final layer of aluminum on top of the transparent oxide to reduce series resistance and better mimic real devices.



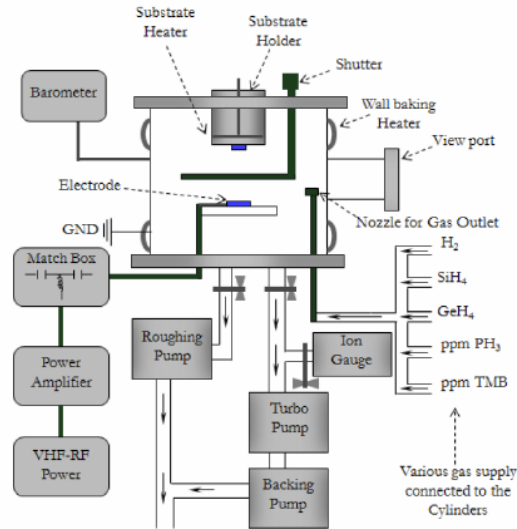
**Figure 2-1. A layer-by-layer diagram of a-Si:H solar cells. Glass encapsulation is not used in this study.**

### 2.1 Plasma-enhanced Chemical Vapor Deposition

Samples were created using plasma-enhanced chemical vapor deposition (PECVD) in a single chamber reactor. A schematic of the CVD reactor is given in Figure 2-2. The system is basically broken down into three main subsystems: (1) The vacuum pumping system to get the chamber to low pressures, (2) the electrical system which supplies power to generate a plasma, and (3) the gas manifold which controls the flow of precursor gases into the reactor.

The vacuum system consists of three pumps and a few sensors. The goal of the system is to get the chamber down to high vacuum as low as  $10^{-7}$  Torr. A mechanical rough pump is used to get the reactor below 1 Torr starting at atmosphere. At that point, a turbomolecular pump is used to further evacuate the reactor chamber down to pressure. Finally, a backing pump is used with the turbo pump to reduce the intermediate pressure.

Standard samples are made at a pressure of 100mT with a substrate temperature of 300°C. Pressures were experimented down to 25mT with temperatures up to 450°C as part of this study.



**Figure 2-2. Schematic of the plasma-enhanced chemical vapor deposition reactor.**

The electrical system consists of a impedance matching system connected to the RF power supply. The RF power is supplied from a power amplifier connected to a signal generator. A RF frequency of 45MHz is the typical value used during deposition. Power values for the intrinsic region vary around 5-8W.

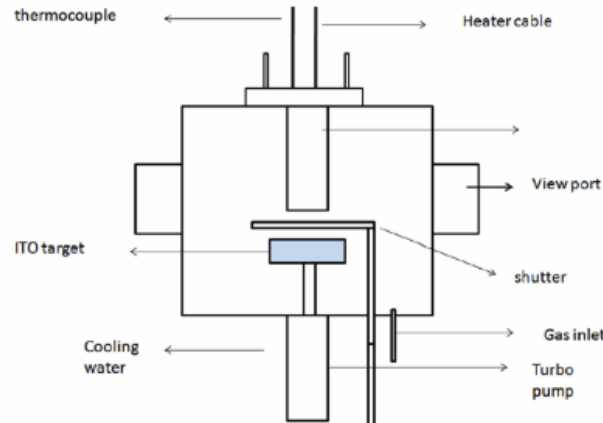
The gas manifold supplies gases to the reactor. The main precursor gases used to deposit hydrogenated amorphous silicon via CVD are hydrogen ( $H_2$ ) and silane ( $SiH_4$ ) in a flow ratio around 10:1. Dopant gases include diborane ( $B_2H_6$ ) and trimethylborane (TMB) for p-type and phosphine ( $PH_3$ ) for n-type. Finally, methane ( $CH_4$ ) is used in the p+ layer to increase the band gap to create a good window layer.

To create the device, the n+ layer is first deposited on a stainless steel substrate using silane and phosphine. The n+ region is typically made to be around 0.25 $\mu m$  thick. Next is the i-layer which is 0.25 $\mu m$  to 0.35 $\mu m$  thick depending on deposition conditions and time.

As the i-layer is deposited parts per million levels of dopants are graded to aid in carrier collection. Methane is also graded towards the p+ layer to match its larger band gap. To finish the PIN structure, a thin (30nm) p+ layer is deposited.

## 2.2 Sputtering of Indium Tin Oxide

After deposition of the PIN layers, the anode made of indium tin oxide (ITO) is deposited using physical sputtering. Figure 2-3 shows a schematic of the sputtering system used to deposit a layer of ITO on top of each cell. ITO acts not only as a conducting anode, but also a transparent window for visible light. In addition, the thickness of the layer is chosen to be approximately a quarter wavelength in thickness at ~70nm to reduce external reflection in the green wavelengths. Sputtering is done in argon plasma at 5mT pressure with a temperature of 225°C and 90W of forward power.



**Figure 2-3. Schematic of the RF sputter system used to deposit ITO. This layer acts as the transparent anode for each sample. Argon atoms in plasma bombard an ITO target, sputtering a layer of ITO on the device.**

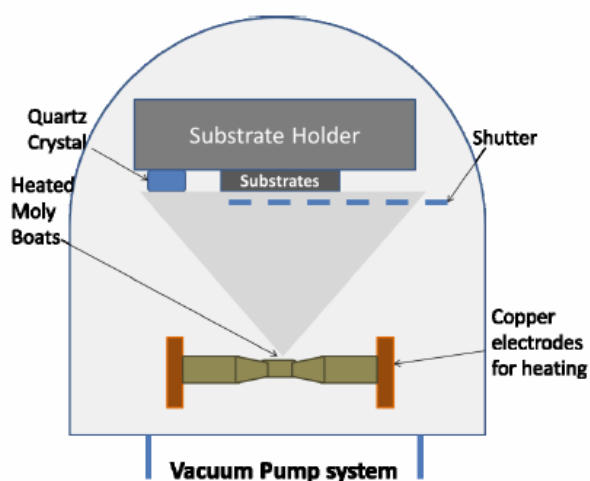
## 2.3 Aluminum Evaporation

For samples undergoing the light soaking process, a layer of aluminum is deposited on top of the ITO layer. Aluminum has a larger conductivity than ITO so series resistance in



the cell is reduced, helping improve fill factor. The extra aluminum bar allows for good contact to be made with probes without adding additional uncertainty due to shadowing.

The process of aluminum deposition is done with thermal evaporation in a vacuum environment. The material comes from aluminum wires which are placed in boats attached to copper electrodes. Voltage is applied to the electrodes, providing enough current to heat the resistive boat until the aluminum melts. At this point the gaseous aluminum rises to be deposited on the samples mounted above. A quartz crystal nearby is also coated, changing its resonant frequency, thereby allowing the deposition thickness to be monitored. For all samples, the thickness of aluminum was kept around 200nm.



**Figure 2-4. Schematic of evaporation system used to deposit aluminum on samples prior to degradation.**

## CHAPTER 3 - DEVICE CHARACTERIZATION

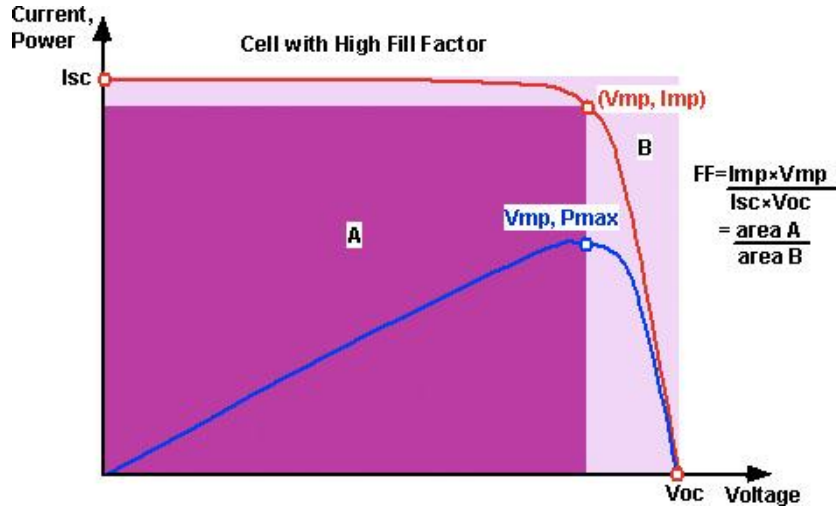
For each sample fabricated, a few standard measurements are conducted to characterize the device. This data is analyzed to determine whether a given device is chosen to go through further testing. Bad devices are studied for their bad properties to improve the characteristics of devices in later fabrication. The best devices are exposed to light and studied for their degradation. The difference between good and bad devices will be described in each measurement with typical data that is expected.

### 3.1 Current versus Voltage

The most commonly reported measurement for solar cells is current versus voltage (I-V). For solar cells, voltage is positive and current is negative from anode to cathode when using the standard method of circuit analysis. By finding the current versus voltage relationship, many important device properties can be determined including fill factor and efficiency.

Fill factor is the ratio of the max power output to the product of short-circuit current and open-circuit voltage. It is roughly a measure of how well carriers are collected in the cell as a function of voltage. The more “square” the curve, the more current that is extracted at a given voltage. This value can never be 100% but above 60% is good in samples made of amorphous silicon. Figure 3-1 shows this feature more clearly.

$$FF = \frac{P_{MAX}}{V_{OC}I_{SC}} = \frac{V_{MP}I_{MP}}{V_{OC}I_{SC}} \quad (3-1)$$



**Figure 3-1. I-V Curve of a Solar Cell in the fourth quadrant.**

Power conversion efficiency (PCE) is the most important value in photovoltaics. This percentage reveals how well electrical power is generated from the incident light power of the sun. To find efficiency from the other determined values, equation 3-2 is used.

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OC} I_{SC} FF}{P_{IN}} \quad (3-2)$$

From the equation, PCE is proportional to short circuit current, open circuit voltage, and fill factor, indicating larger is better in all three values. Unfortunately, open circuit voltage is a function of band gap which limits the portion of the solar spectrum which can be absorbed. The larger the band gap, the fewer photons which can be absorbed which reduces current density. Thus, there is a bit of a tradeoff between these values as will be looked at later on with our study. With the reactor and facilities used for this study, good devices have PCE over 6%.

To collect data, probes are connected to the anode and cathode (substrate) and voltage is swept while current is measured. This is done with a computer and a Keithley 236 source-measure unit (SMU). The software first measures the open circuit voltage and short circuit current by applying 0A and 0V respectively while measuring the reciprocal value. Using the

open circuit voltage, a starting voltage is calculated for the sweep. 125 points are taken in evenly spaced intervals from the starting voltage to -0.5V while measuring current at each point. Upon completion of the sweep, the maximum power point is found in the array and used to calculate fill factor. Finally, by using fill factor, efficiency can be calculated (Eqn 3-2).

### 3.2 Quantum Efficiency and QE Ratio

The measure of the efficiency for cells to collect charge carriers is given by a property called quantum efficiency. External quantum efficiency (EQE) is the ratio of the number of collected carriers (electrical current) to the incoming number of photons. It is typically measured at a given wavelength using a light source with a monochromator. Internal quantum efficiency (IQE) takes account for external reflection and is the ratio of collected carriers to the number of electron-hole pairs generated. Both are important but EQE tells the real story of how well photons are being converted to electrical current in a device.

$$EQE = \frac{\# \text{ of Collected Carriers}}{\# \text{ of Incident Photons}} \quad (3-3)$$

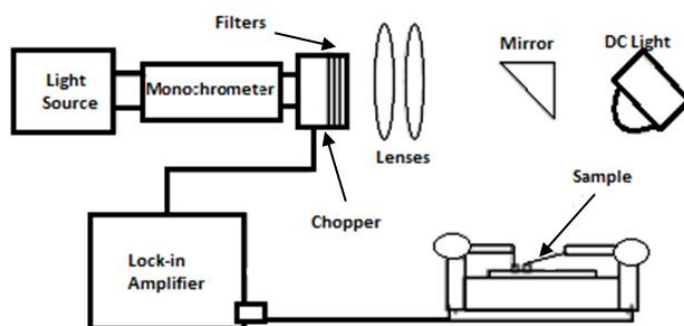
The main signature of large EQE is a large current density in the cell. The integration under the EQE curve gives the current density of a device based on equation 3-4 where  $\phi_{ph}$  is the photon flux from the sun at a given energy (wavelength).

$$J_{sc} = q \int QE(E) \phi_{ph}(E) dE \quad (3-4)$$

The schematic for the setup for measuring EQE is given in Figure 3-2. A light source is made into a narrow range of frequencies (wavelengths) using a monochromator. The light is then passed through a chopper that spins at 13Hz. This frequency of rotation allows for the

use of a lock-in amplifier to detect the small signals typical of these measurements. The light then goes to either the sample or a reference photodiode made of crystalline silicon. By comparing the generated current from the sample to the current and known EQE for the photodiode, the EQE can be found for any wavelength.

Electrically, probes are connected to the samples which are connected to a pre-amplifier that converts current into voltage. This voltage signal then goes to the lock-in amplifier which detects the 13Hz signal and amplifies it to be measured. Thus, the monochromator can be used to sweep wavelengths while taking measurements of the lock-in amplifier to determine EQE. An example of EQE data is given below in Figure 3-3. Measurements are normalized to a ratio of 0.9 at the maximum wavelength and then changed absolutely to match the current density measured from the I-V data.

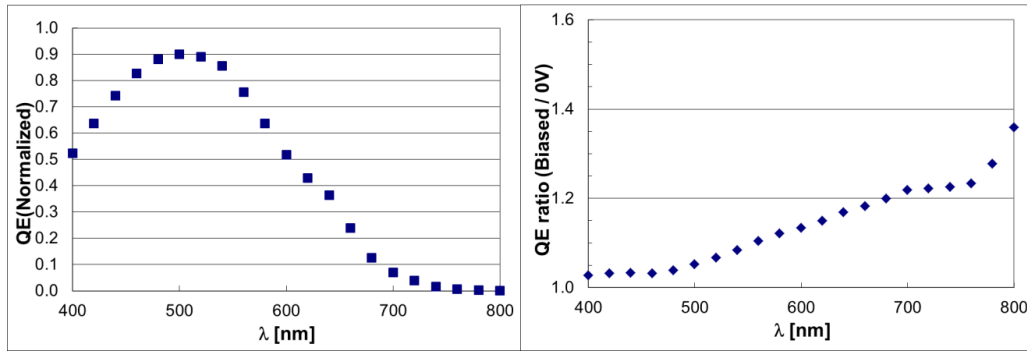


**Figure 3-2. Block-level schematic of the EQE measurement setup.**

Typically QE is measured without electrical bias. Light bias is included though to provide a DC signal on which the 13Hz signal is superimposed. By taking the ratio of QE when the cell is biased at +0.5V and at zero bias, further information about carrier collection can be extracted. At positive bias, the depletion region has been decreased so carrier collection will decline as discussed in Chapter 1. If this decline is low then this indicates that carrier collection is not a function of bias but rather charge carriers are easily collected using only the built-in field provided by the junction. Since this collection can be probed with

changing bias, the  $\mu\tau$  (mu-tau) product can be found by sweeping voltage and measuring EQE at a single wavelength, usually above 700nm where hole collection decreases.

Two key features of QE ratio are of importance in most cases. At low wavelengths below 500nm, QE ratio often starts high and declines monotonically towards 500nm. Since this is in the region of well absorbed photons, the negative slope indicates a poor interface between the P and I layers. Oppositely, a positive slope at wavelengths above 600nm indicates collection issues for the minority carriers. Sample data is given in Figure 3-3 which shows a sample with very poor hole collection.



**Figure 3-3. Sample data from EQE measurement along with measurement for QE ratio.**

### 3.3 Defect density using capacitance measurements

Knowledge of defects in a-Si:H solar cells is vitally important since the amount of disorder has an effect on carrier mobility and recombination. In addition, light-induced degradation has been shown to relate to defects in the cell so studying the defects can show which cells are likely to degrade the least and what is happening during degradation. To probe these defects, capacitance spectroscopy is used with both capacitance versus bias and capacitance versus frequency measurements.

The theory of capacitance versus voltage measurements is based on the typical diode theory in which a PN junction forms a depletion region separating two regions where carriers

are prevalent. The behavior is similar to a parallel-plate capacitor with a relationship that depends on applied voltage. Equation 3-5 gives this relationship where  $V_R$  is applied reverse bias and  $N_{SCR}$  is the charge in the region.  $V_0$  is the built-in voltage of the junction.

$$\frac{C}{A} = \frac{1}{2} \left[ \frac{2q\epsilon}{V_0 + V_R} N_{SCR} \right]^{1/2} \quad (3-5)$$

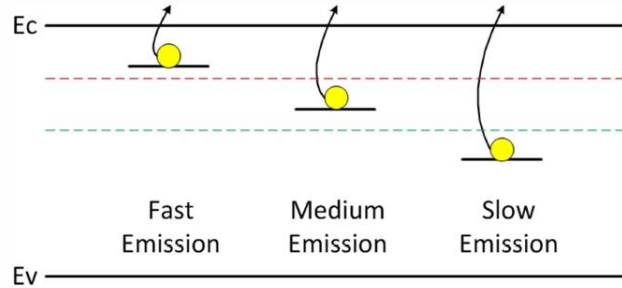
Obviously,  $C/A$  has an inverse square relationship to the applied reverse bias. By plotting  $(A/C)^2$  versus  $V_R$  the value of  $N_{SCR}$  can be extracted from the slope. According to Kimerling, defects also impact this measurement in addition to free carriers especially when the frequency of applied voltage in the capacitance measurement is much less than the emission rate of those traps [18]. By measuring capacitance versus frequency at low frequencies (20Hz) and at elevated temperatures (150°C), the trap states are very active and the slope of the plot of  $(A/C)^2$  versus  $V_R$  gives the total number of defects in the band gap. In other words,  $N_{SCR} \approx N_T$  assuming the number of traps is much larger than other defects in the intrinsic layer.

Measuring capacitance versus frequency gives a defect profile based on theory by Walter et al [19]. Figure 3-4 summarizes this work and how it applies to capacitance measurements. Using Equation 3-6, a defect profile of  $N_T$  versus trap energy can be found by taking capacitance measurements at different frequencies  $\omega$ . In this formula  $U_d$  is the built-in voltage of the junction and  $W$  is the depletion width assumed to be the i-layer thickness.

$$N_T(E_\omega) = \frac{-U_d}{qW} \frac{\omega}{kT} \frac{dC}{d\omega} [cm^{-3}eV^{-1}] \quad (3-6)$$

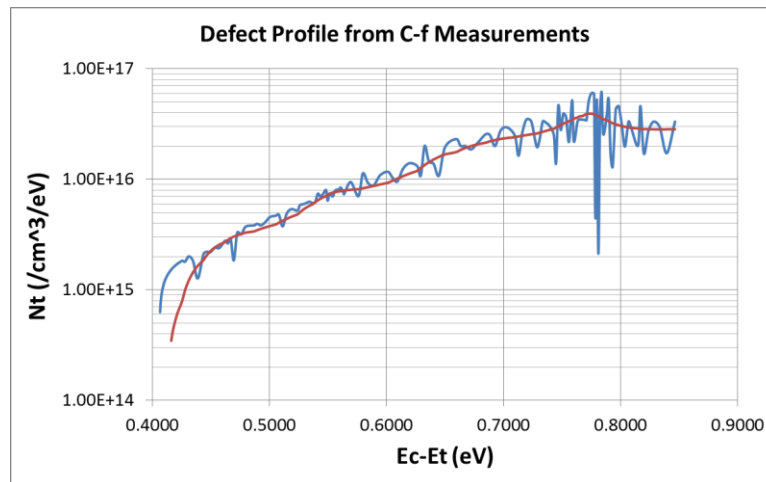
Due to the differential term in the equation, the noise from the measurement of capacitance is amplified. To remove this noise in the defect profile, wavelet analysis is performed with MATLAB software. The upper frequencies are removed, smoothing out the

profile. In Figure 3-5, a sample result is presented. The blue line is the initial data from equation 3-6 while the red curve is the denoised result.



**Figure 3-4. Diagram of Trap Emission. Fast emission states are shallow states and can be detected at high frequencies. For slower emission traps, measurements must be done at lower frequencies. By varying frequencies while taking capacitance measurements a profile of these defects can be created [20].**

C-f and C-V measurements have been used often within our group applied to other non-crystalline semiconductors like nanocrystalline silicon and organic electronics in addition to amorphous silicon. For further explanation of this measurement please read the work done by Congreve [20]. To profile all the way to midgap, frequency is swept from 20Hz to 200kHz with no bias voltage and an AC signal of 50mV.



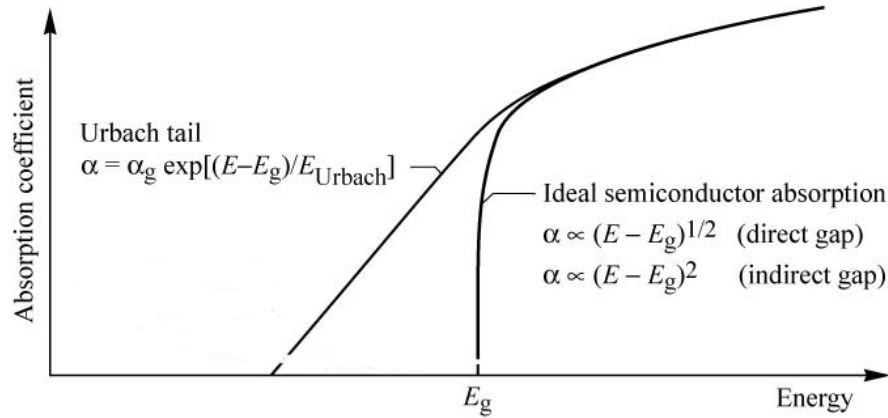
**Figure 3-5. Sample result of capacitance versus frequency measurement showing defect density versus energy difference compared to the conduction band.**



### 3.4 Subgap Absorption

As shown in Chapter 1, the density of states for amorphous silicon includes tail states in the band gap that exist near both band edges. QE at wavelengths above the band gap can be measured to explore these states. Specifically, the tail states near the valence band can be observed since holes are the minority carrier. Since theory shows these states to decay exponentially from the valence band, the measured QE should exponentially decrease as wavelength increases. The reciprocal of the slope of this exponential line gives the Urbach energy, a measurement of the quality of the amorphous film [11]. The best devices have Urbach energies  $\sim 45\text{meV}$  while devices that are not as good are closer to  $60\text{meV}$  although in this study good devices are made that still have a large Urbach energy. Figure 3-6 and Equation 3-7 show how Urbach energy  $E_U$  appears in the absorption coefficient which is directly measured by subgap QE.

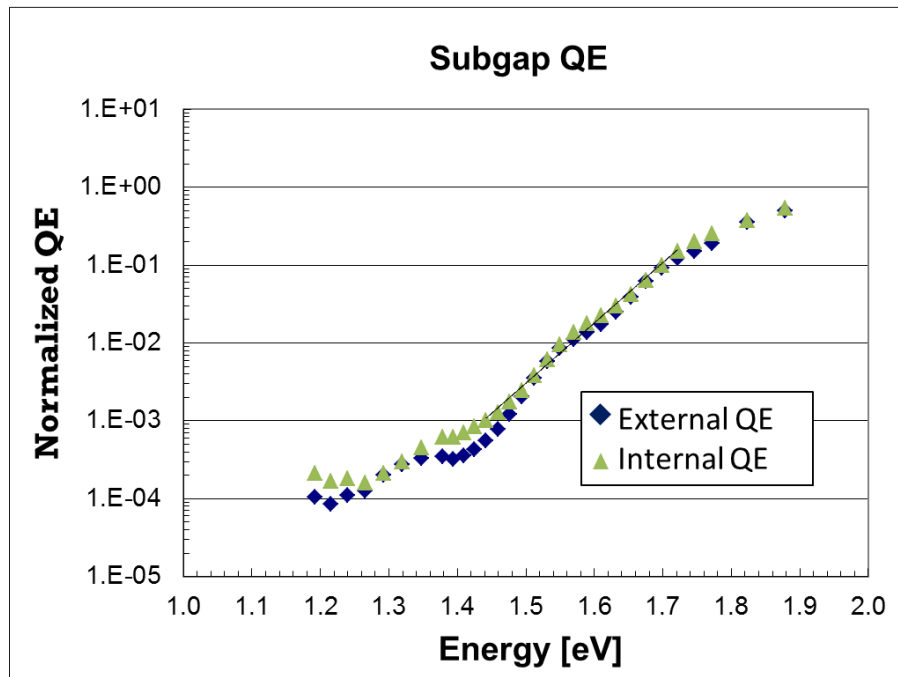
$$\alpha = \alpha_0 \exp(E/E_u) \quad (3-7)$$



**Figure 3-6. Absorption versus energy showing the Urbach tail states that extend from the ideal semiconductor behavior [11].**

The initial measurements of subgap QE are more specifically termed external QE because some of the incident photons do not make it into the cell. Internal QE, on the other hand, measures the efficiency of charge carriers to be collected compared to the number of

photons that are absorbed. Thus, the difference between external QE and internal QE is reflection. Since cells are so thin, on the order of  $0.5\mu\text{m}$ , interference effects show up when measuring external QE. This makes finding the exponential slope difficult. By measuring reflectance and removing it from EQE the curve becomes smoother, making the analysis much easier. Figure 3-7 shows a sample measurement of subgap QE with both EQE and IQE. The IQE curve is much smoother, making analysis easier. In this study, Urbach energy is compared before and after light exposure to investigate how the valence band tail states are changing over time.



**Figure 3-7. Typical result of subgap QE measurement. The exponential slope of the IQE line indicates the Urbach energy which is related to the quality of the a-Si:H film.**

### 3.5 Device Thickness

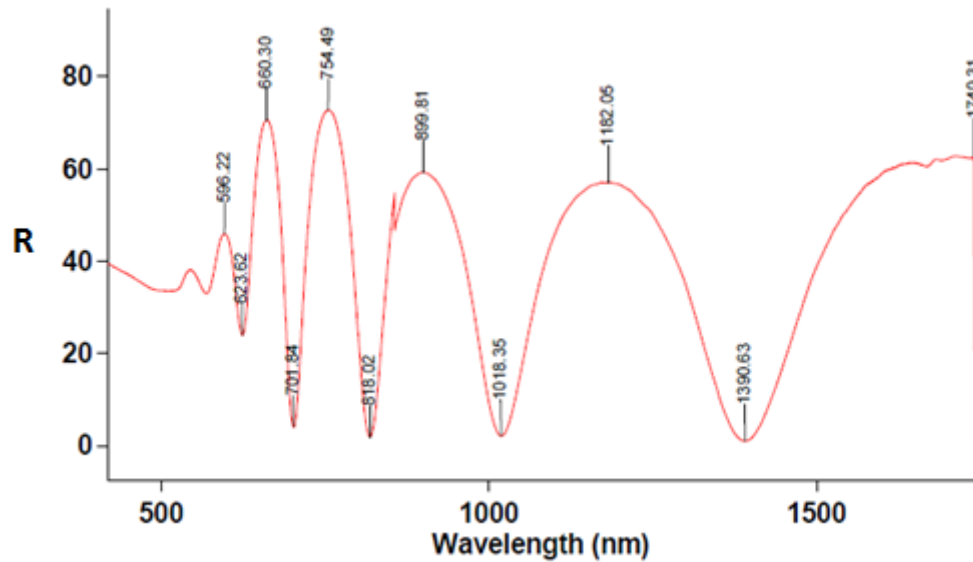
To tune fabrication and make connections to other variables, sample thickness is measured. The method of measuring thickness is based on thin-film spectroscopy, specifically on the diffraction effects that exist when dielectric layers have thicknesses near

the wavelength of light. Since the a-Si samples were around 0.5 $\mu\text{m}$  thick, this condition is readily met.

The measurement is done with an Ocean Optics setup. Light is shone on a sample while measuring reflectance. The reflectance spectrum consists of many peaks and valleys. The wavelength where these maxima and minima occur is a function of cell thickness based on Equation 3-8 from Swanepoel [22]. In this equation,  $\lambda_1$  and  $\lambda_2$  are the wavelengths of two consecutive maxima or minima in the reflectance (or transmittance) curves with  $n_1$  and  $n_2$  being the refractive indices at those wavelengths. As thickness increases, the separation between maxima/minima decreases until the oscillations are no longer discernible.

$$d = \frac{\lambda_1 \lambda_2}{2(\lambda_1 n_2 - \lambda_2 n_1)} \quad (3-8)$$

Figure 3-8 below shows reflectance data from an a-Si solar cell. Based on this data, the calculated thickness is 0.57 $\mu\text{m}$ . One assumption that is made for the thickness calculation is that the material has a band gap energy of 1.8eV. As is shown in Chapter 5, this assumption may not be correct when varying fabrication temperature.



**Figure 3-8. Sample data of reflectance used for measuring sample thickness.**

In addition to total thickness, the thickness of the intrinsic layer is also desired. This is done using capacitance spectroscopy. The voltage in reverse bias at which capacitance saturates marks the point where the intrinsic region is completely depleted of carriers. By using the traditional Mott-Schottky diode theory, the thickness of the intrinsic layer can be determined by Equation 3-9.

$$W = \frac{Area * \epsilon_s}{C_{depletion}} \quad (3-9)$$

Since the drift (range) of carriers is decreased with a thicker intrinsic layer, this value is important to keep degradation low. Thinner intrinsic layers are impervious to degradation because the built-in electric field is always large enough to collect carriers (refer to Chapter 1). All devices studied had an intrinsic layer between 0.25 $\mu$ m and 0.35 $\mu$ m.

## **CHAPTER 4 - DEGRADATION SETUP AND MEASUREMENTS**

Taking only the best samples, light soaking was conducted using an experimental apparatus that was designed, built, and operated at Iowa State University's Microelectronics Research Center. This chapter describes the motivation for the system and describes the design.

### **4.1 Specifications**

Initial measurements on this project were done with an ELH halogen lamp connected to our standard I-V setup. Thus, the I-V curve was taken automatically by software but measurements over time required manually showing up to change wires and start the sweep. Every 5-10 hours measurements were needed, which required precise scheduling to not interfere with other events. Thus, data throughput was restricted and reduced. What was needed was an automated, in-situ measurement of degradation over time. In addition, a better light source was needed to better match the spectrum of the sun. The specifications of the setup were as follows:

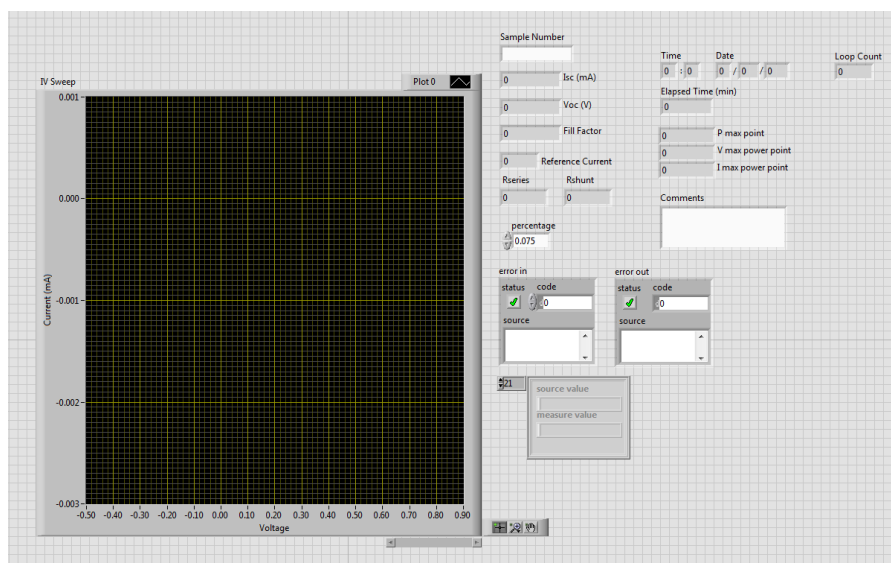
- Stable light source with AM1.5 spectrum that can last over 100hrs per bulb.
- In-situ I-V measurements taken automatically at defined periods for 100+ hours.
- Exposure of samples at 2x intensity with measurements taken at 1x solar intensity.
- Reference photodiode with known characterization for monitoring the stability of the light source over time.
- Software to control everything automatically so there is no user interaction required over the time frame of the measurement.
- Automatic calculation of important values and creation of data files to store all raw data for future analysis.

### 4.1.1 Light Source

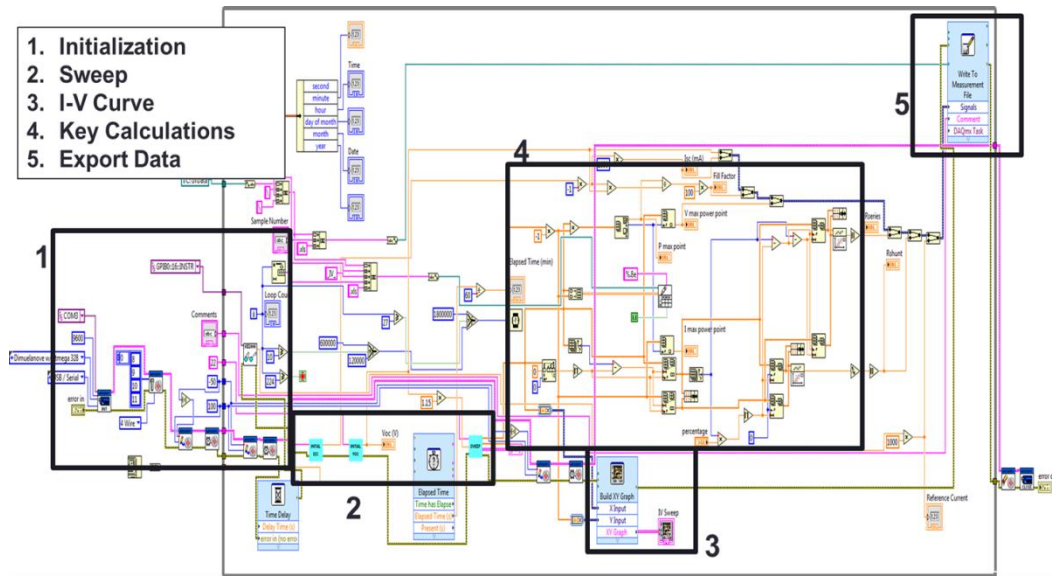
The lighting requirements were met with an ABET 10500 solar simulator. The simulator uses a Xenon arc lamp and optical filters to match the standard AM1.5 spectrum as defined by the American Society for Testing and Materials [23]. This source produced a light intensity of one times sun intensity at an 18" optical length with a circular light area of around 35mm diameter. The light source intensity was measured prior to each measurement with a standard c-Si photodiode to confirm intensity.

### 4.1.2 LabVIEW Program

To automate the control of all components, a LabVIEW program was created that takes advantage of the GPIB interface common in most characterization devices. Figure 4-1 shows the graphical user interface while Figure 4-2 shows the final program with the main parts of the program highlighted by functionality. The user is only required to provide a sample number and any desired comments before pressing start. The measurements are taken automatically at periods defined by the program which can be adjusted if needed.



**Figure 4-1. GUI for the light soaking program. Program is made to be user-friendly and is highly autonomous so little interaction is required until the exposure time has elapsed.**



**Figure 4-2. Block-level diagram of the LabVIEW light exposure program. The diagram highlights the program's major parts.**

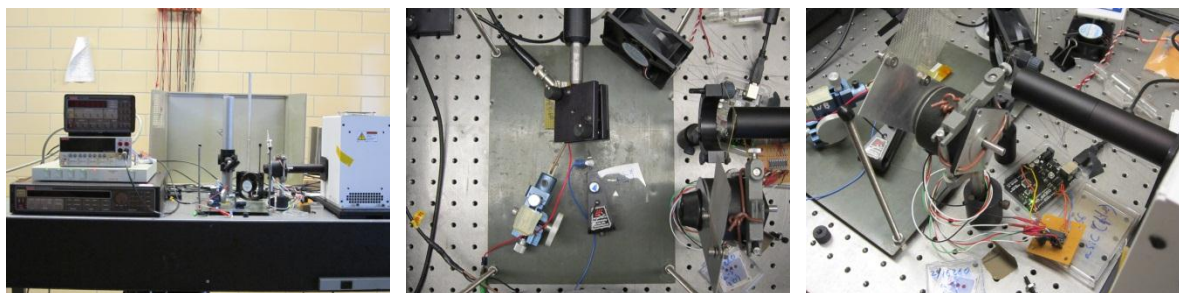
#### 4.1.3 Motor Controller

It was desired to accelerate degradation by exposing each sample to 2x sun intensity while measurements would still be taken at 1x intensity. To do this a 50% optical mesh was used to cut light intensity by half when placed in the light's path. With the use of a stepper motor attached to the mesh and connected to an Arduino microcontroller, the same LabVIEW program was able to control light intensity autonomously. Before each measurement the stepper motor moved the mesh into the light path. Afterwards, the mesh was removed to allow the light exposure to continue at two times sun intensity. The stepper motor was connected to a simple motor driver IC which was tied to the digital outputs of an Arduino microcontroller. The microcontroller was connected via USB to the computer and interfaced with the same LabVIEW program to insure synchronized operation.

#### 4.2 Completed Degradation Setup

Figure 4-3 shows pictures of the completed setup. The left most image is of the entire setup located on an optical table for precise alignment of items. The middle image is an

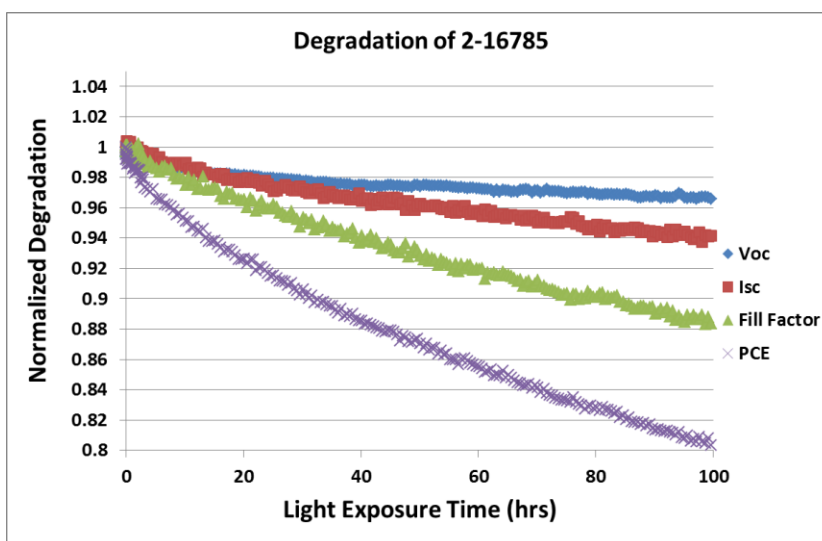
overhead view of the sample stage. A mirror reflects light from the source to the sample. A fan near the rear of the stage keeps samples near 300K. The final image shows the stepper motor connected to the optical mesh with the motor driver and microcontroller located below.



**Figure 4-3. Light soaking setup used to measure solar cell degradation in-situ.**

### 4.3 Example Results

To prove the operation of the apparatus prior to further studies, sample data was taken and compared to the data taken with the ELH Halogen setup. Figure 4-4 shows data for a standard sample with typical degradation behavior. Notice that a data point is taken on average every 30 minutes compared to every 5-10 hours with the previous setup.



**Figure 4-4. Example data from an a-Si:H sample using the degradation setup and program.**



## CHAPTER 5 - RESULTS

### 5.1 Standard Samples

The control devices were made of a standard recipe that is used to calibrate our CVD reactor. While the n+ and p+ layers are similar for all samples in this study, the fabrication of the all-important intrinsic layer is altered. Standard devices are made at a measured electrode temperature of 300°C at 100mT. The lower intrinsic layer (I2) is deposited for 35 minutes with a power around 7.5 watts. This results in an intrinsic layer thickness of 0.3μm. Typical characteristics are outlined in Table 5-1 for the sample shown as the “Standard” device in the remainder of chapter 5 and 6.

**Table 5-1. Solar cell parameters for a typical standard sample which is used as the control device.**

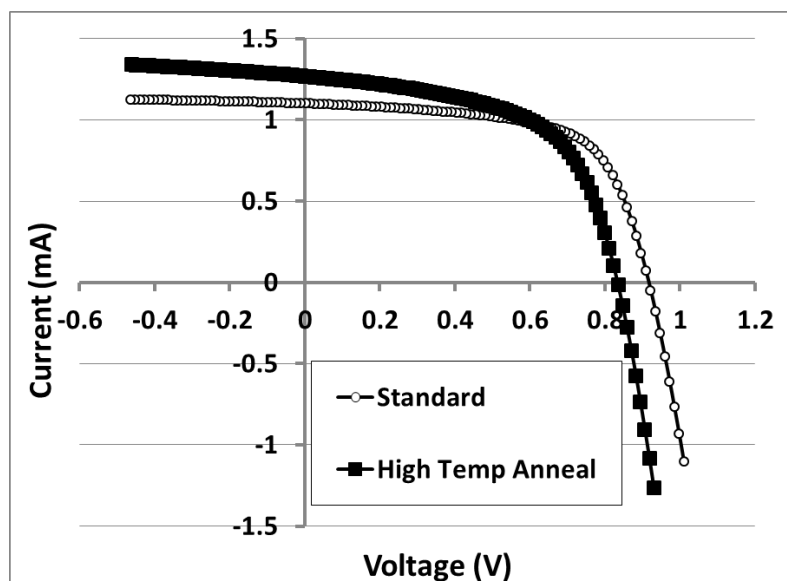
Cell Parameter	Value
V <sub>oc</sub>	0.918 V
I <sub>sc</sub>	1.10 mA
Fill Factor	64.7%
Power Conversion Efficiency	5.23%

### 5.2 High Temperature Anneal

Based on the research of at NREL (see Chapter 1), high temperature annealing of hydrogenated amorphous silicon thin films reduces the number of dangling bonds that are measured after light exposure [17]. The thought was that light-induced degradation could be reduced by using this idea to fabricate a-Si:H solar cells.

To fabricate these devices, the standard fabrication was done to create the n+ and intrinsic layers. After finishing the intrinsic layer, the sample was heated to elevated temperatures up to 425°C in a hydrogen atmosphere for up to 60 minutes. Annealing times

over 20 minutes did not have much of a difference and devices were marginal in quality. Figure 5-1 shows a comparison of current versus voltage measurements for a device made by high temperature annealing of the intrinsic region and the standard sample.

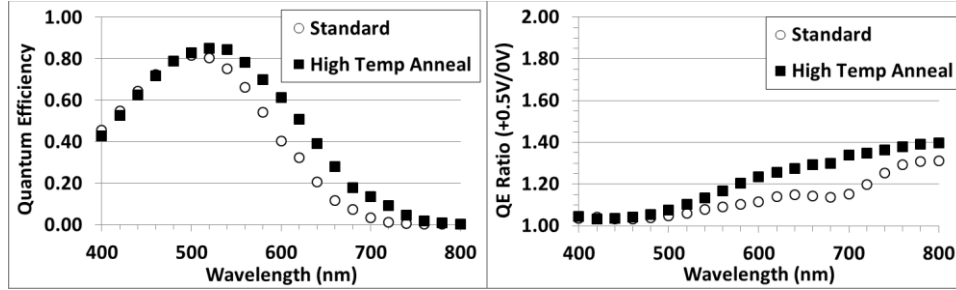


**Figure 5-1. I-V curves for samples created with a high temperature anneal step compared to the standard device. Fill factor is 57.8% indicating poor carrier collection.**

Table 5-2 below shows the initial I-V characteristics for six devices made using this high temperature anneal method. The third device is the only device that did not include boron grading as described in the next section. Notice that currents are larger but voltage is lower compared to standard samples. More importantly, fill factor is far lower at 57.8% indicating poor collection.

Quantum efficiency measurements are given in Figure 5-2 once again comparing the standard device to the same high temperature annealed device. The QE plot shows that the wavelength of maximum absorption is shifted to the red due to a smaller band gap due to the elevated fabrication temperature. This results in a larger current density due to a larger photon flux at the green wavelengths. The consequence of a smaller  $E_g$  is a smaller open-circuit voltage. The QE measurements also show a QE ratio that is worse for the annealed

device in the longer wavelengths. At 800nm, the standard device has a ratio of 1.3 while the ratio for the annealed sample is almost 1.4. From 600nm onward, the annealed device has a higher ratio. This indicates poor hole collection, partly explaining the low fill factor in the I-V curve. Thus, simply annealing devices does not produce solar cells with acceptable performance even before degradation.



**Figure 5-2. Quantum efficiency and QE ratio of a sample annealed at elevated temperatures compared to a standard sample.**

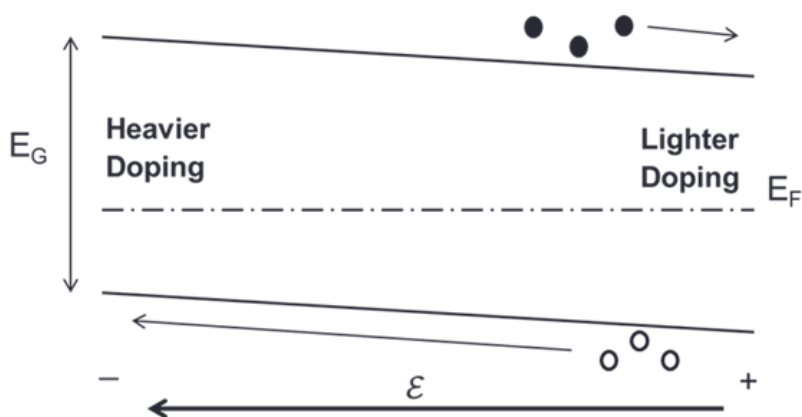
### 5.3 Gradient of Doping with Boron

To improve these devices to an acceptable efficiency, fill factor needed be increased. In amorphous silicon, the main driving force that allows photo-generated carriers to be collected is the built-in electric field created by the separation of Fermi levels between the p+ and n+ layers as discussed in Chapter 1. By adding a gradient of dopants, this built-in field can be augmented according to Equation 5-10 assuming the doping changes the density of holes [24]. See Figure 5-3 for an energy band diagram of this effect.

$$\mathcal{E}(x) = \frac{D_p}{\mu_p} \frac{1}{p(x)} \frac{dp(x)}{dx} \quad (5-1)$$

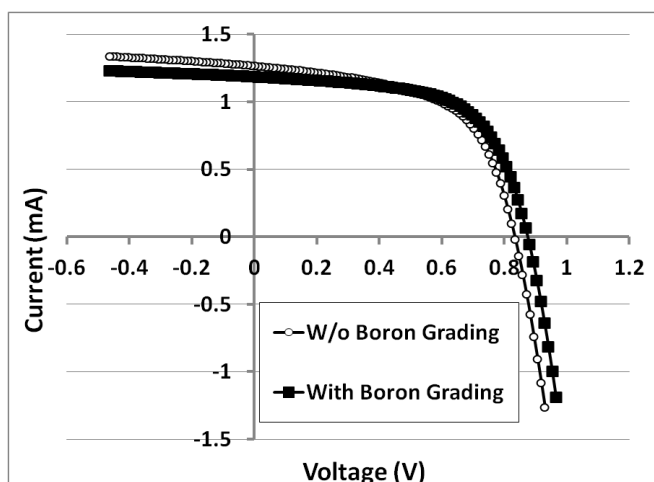
A gradient of doping is also used to aid with degradation. Since it is suspected that the addition of light-generated defects decreases the built-in field over time (Figure 1-6), the idea is to add a parts per million gradient of boron using trimethylborane (TMB) to supplement the built-in field that already exists. The gradient is made during growth of the

intrinsic layer by slowly increasing gas flow of TMB. This is only done for the first 5-10 minutes of i-layer growth. Then, TMB is kept constant until the layer is finished.



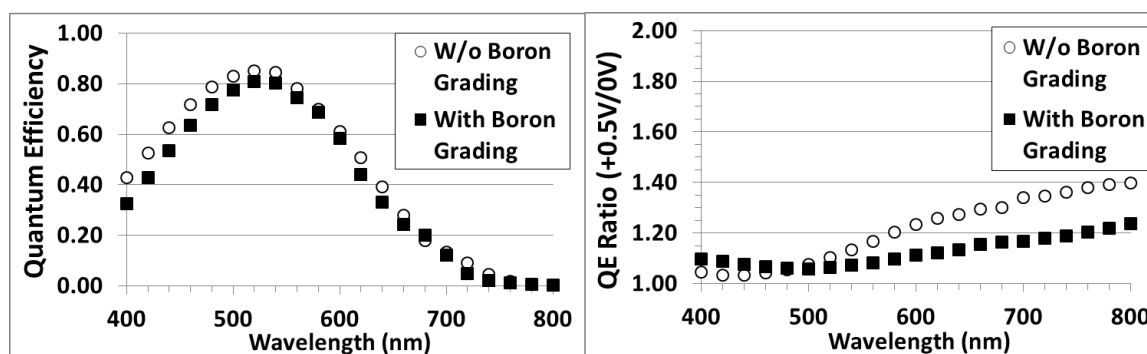
**Figure 5-3. Energy band diagram of the intrinsic layer with ppm boron grading. The gradient of dopants produces a built-in electric field which enhances carrier collection.**

Below in Figure 5-4 is the I-V curve of a sample made with boron grading compared to a similarly prepared sample with constant doping in the intrinsic layer given previously. All other conditions were kept the same. Fill factor is indeed improved from 58% to 62%. With the addition of aluminum to reduce series resistance, fill factor increases to 65%. All devices from this point onward use a gradient of boron doping in the intrinsic layer in order to increase fill factor and reduce degradation to some extent. The magnitude of the gradient and the end points were varied to optimize the best device at each fabrication condition to get the best initial cell. Too much TMB decreases  $\mu\tau$  while too little does little to add to the built-in electric field that needs to be increased.



**Figure 5-4. I-V comparison between samples with and without TMB grading in the intrinsic layer. Notice the much better fill factor from the sample using boron grading.**

Figure 5-5 shows the comparison of the QE measurements between the device with TMB grading and one without. For the two devices, QE is similar although slightly lower for the device with boron grading due to a slightly thinner i-layer. The QE ratio shows that holes are collected well at all wavelengths for the TMB graded device with the largest ratio being 1.2 at 800nm, which is much lower than for the sample without TMB grading.



**Figure 5-5. QE comparison between samples using boron grading and those without.**

Table 5-2 gives an overview of a few devices created using a high-temperature anneal of the intrinsic layer. The table includes devices that do and one that does not include TMB grading. At the bottom is the standard device for comparison. As discussed before, compared to the standard sample, the voltage of these samples is decreased due to a lowering of the band gap at elevated temperatures. This assists in absorbing more of the spectrum,

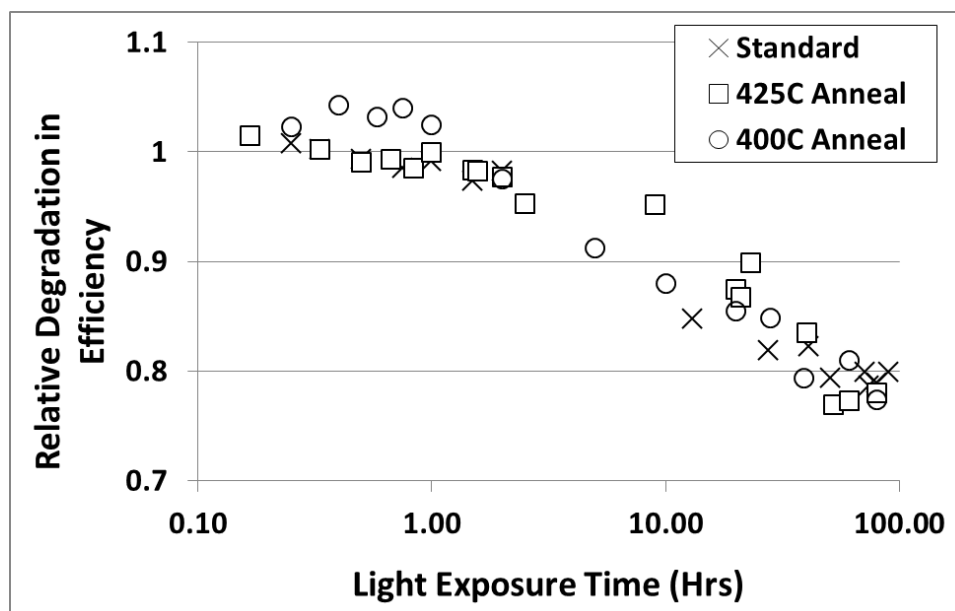
resulting in larger short-circuit current densities. Fill factors for the devices using boron grading are mostly >60% whereas the fill factor for the device without is around 58%.

**Table 5-2. Initial characterization of devices made by annealing at high temperatures.**

Anneal Temp.	Boron Grading	V <sub>oc</sub>	I <sub>sc</sub>	FF
400°C	Yes	0.868V	1.12mA	61.2%
400°C	Yes	0.871V	1.32mA	61.6%
425°C	NO	0.834V	1.27mA	57.8%
425°C	Yes	0.834V	1.27mA	61.2%
425°C	Yes	0.842V	1.32mA	59.3%
425°C	Yes	0.861V	1.23mA	60.3%
Standard	-	0.918V	1.10mA	64.7%

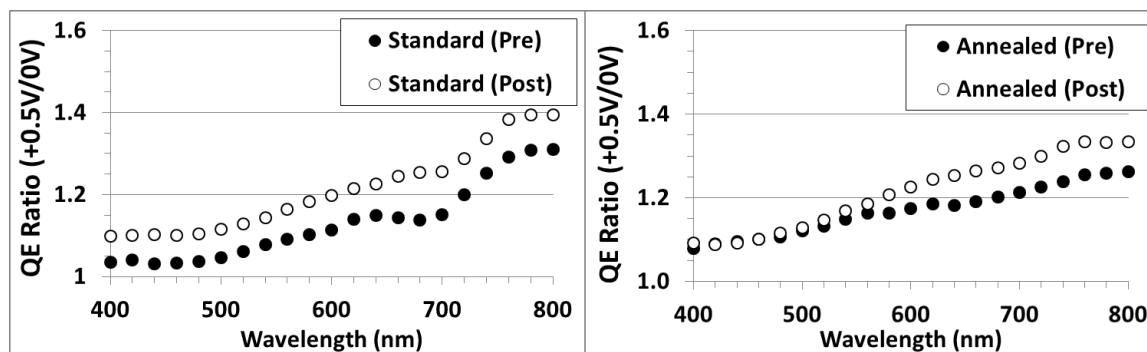
#### 5.4 Degradation of Devices Annealed at High Temperatures

Two of the best annealed devices were exposed to light at two times sun intensity. Current vs. voltage measurements were taken periodically with the degradation setup at normal intensity. Efficiencies were calculated assuming 100mW/cm<sup>2</sup> intensity and compared to the initial measurement. Figure 5-6 gives the results. For all three devices, the degradation in efficiency after 100 hours of light exposure was nearly the same around 20%. In fact, looking closely, the annealed devices actually degraded slightly more than the standard sample. Since these devices started out with less satisfactory efficiency and degraded similarly, evidence shows this method of a-Si:H solar cell fabrication is undesired. The conclusion was made that the work of Stradins et al at NREL does not apply well to solar cells, at least directly.



**Figure 5-6. Degradation of power conversion efficiency for two annealed samples compared to the standard sample. Measurements show that all three degrade by nearly the same amount.**

In Figure 5-7, the QE ratios from before and after degradation are presented for the high temperature annealed sample and the standard device. In both cases, the ratio increased after the sample was exposed to simulated sunlight. The effect is most prevalent at the longer wavelengths but shows up in the shorter wavelengths as well. This seems to confirm the assumption that thickness plays a function in degradation. Recombination centers seem to be created by light throughout the intrinsic layer but the longer wavelengths, which are absorbed deeper in the device, show a larger decline in QE ratio.



**Figure 5-7. QE ratio of standard and annealed samples before and after light exposure.**

## 5.5 Fabrication at High Temperatures

As stated previously, the NREL result applied to solar cells was ineffective at creating more stable devices. It was suspected that the stop-and-go nature of the anneal step may have generated defects between the p+ and intrinsic layers which caused poor devices. To alleviate this suspected issue while sticking to the same idea of high temperature fabrication to reduce defects, the rest of the study considered deposition at high temperatures up to 450°C (at the electrode). By doing the entire deposition of the i-layer at higher temperature, the desire was to reduce dangling bonds and other defect voids created when hydrogen is not removed from the deposited layer prior to the next incoming layer of silicon.

Table 5-3 gives a summary of devices made at elevated temperatures with boron grading. For the same reasons as before, the voltages are lower with higher currents. Unlike with the annealed samples, the fill factors are much closer to the same values as that for the standard samples and even higher for one sample. These devices have excellent QE as would be expected. The conclusion is that good devices can be made at high deposition temperatures with minor changes in fabrication.

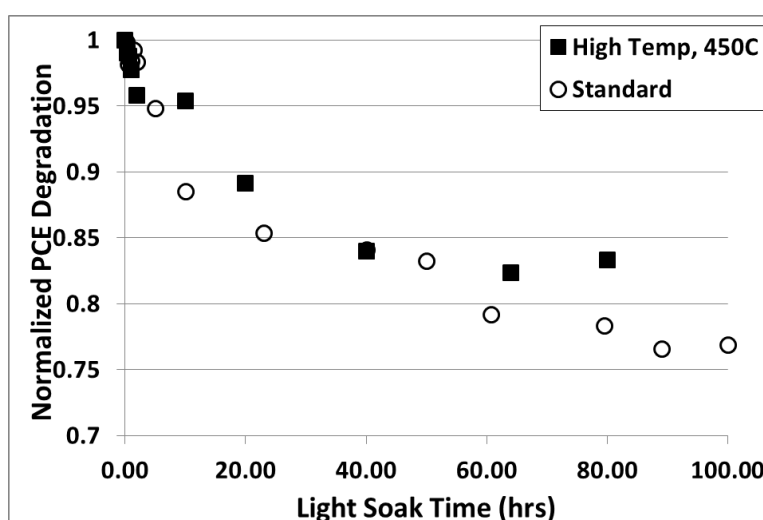
**Table 5-3. Samples created with high temperature growth.**

Growth Temperature	Boron Grading	V <sub>oc</sub>	I <sub>sc</sub>	FF
400°C	Yes	0.890 V	1.04mA	64.1%
425°C	Yes	0.884V	1.06mA	66.3%
450°C	Yes	0.879V	1.06mA	62.4%
Standard	-	0.918V	1.10mA	64.7%



## 5.6 Degradation of High Temperature Samples

After fabrication and normal analysis, the high temperature samples were degraded. The results of the light soaking experiment are shown in Figure 5-8. The figure shows that up to 80 hours of exposure at 2x intensity light the high temperature device degrades less than the standard sample. The degradation for the experimental device was 17% through 80 hours when an error caused the program to halt. At the same point, the standard sample had degraded by 23%.



**Figure 5-8. Comparison between the degradation of the standard sample to a sample fabricated at high temperatures. Degradation is slightly improved for the high temperature sample.**

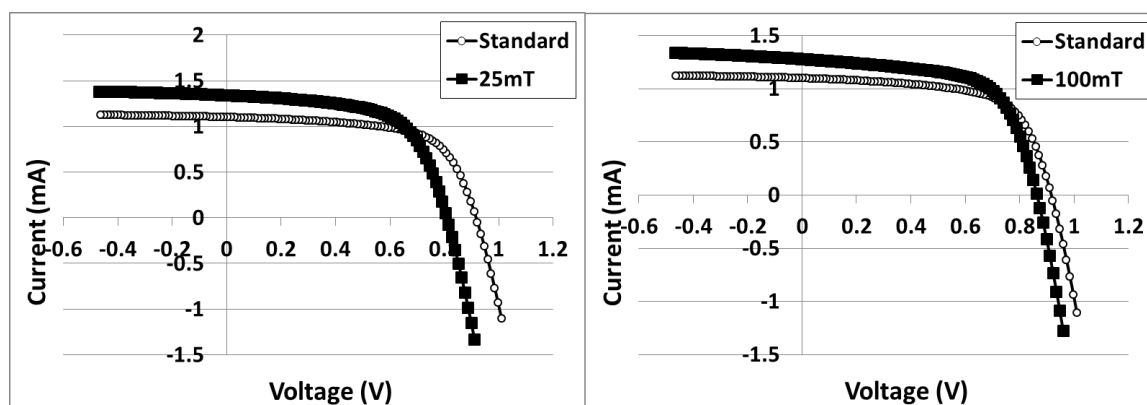
While the results were promising, they did not show as much of a change as was hoped. The study expanded to see how other fabrication adjustments could reduce degradation in combination with high temperature fabrication.

## 5.7 Fabrication at Lower Pressures

As described in Chapter 1, a method used to reduce degradation was to bombard the intrinsic layer with helium ions after growing a thin film of a-Si. The consequence of this method was a much slower time to produce a single cell. The idea was proposed to use

lower pressure deposition to increase the ion energy of the plasma by increasing the mean free path. Since hydrogen is a precursor gas and also used for ion etching of the chamber between steps, the thought was that low pressure and high temperature fabrication would increase the energy that hydrogen atoms had when bombarding the substrate. If these ions could crash with enough energy to break the weaker Si-2H bonds that lead to voids, then degradation could be improved.

Figure 5-9 shows I-V curves of samples created at both 25mT and 100mT as studied previously. The 25mT sample required further changes to keep a fill factor above 60%. Hydrogen to silane gas flow ratios were reduced to only 8:1 compared to 10:1 for the previous samples. This was necessary to keep the hydrogen concentration the same in the sample.



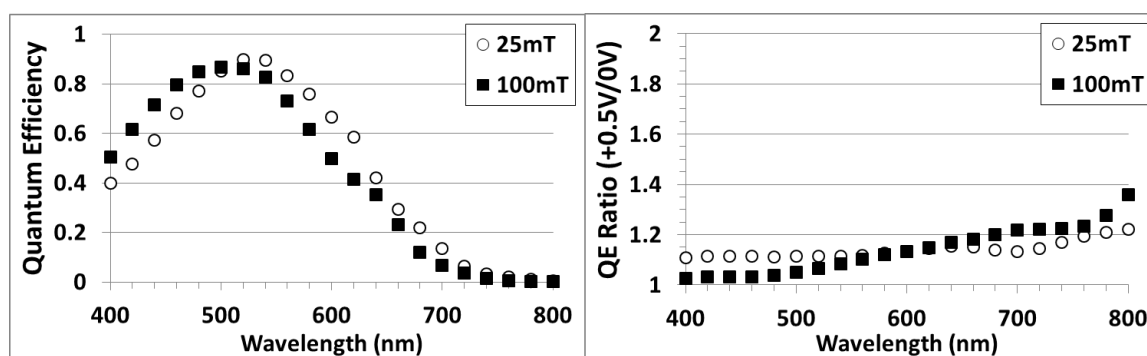
**Figure 5-9. I-V comparison of samples created at 100mT and 25mT both at 450°C.**

Comparing the 25mT to the 100mT sample, the fill factor is less at 63% compared to 64%. Voltage is reduced as the band gap continues to decrease with adjustments to fabrication while short-circuit current is similar. The trend is easier to spot when comparing Table 5-4 of low pressure devices to Table 5-3 of devices fabricated at high temperature only.

**Table 5-4. Samples created with high temperature growth and low pressure.**

Growth Temperature	Pressure	$V_{oc}$	$I_{sc}$	FF
425°C	50mT	0.841V	1.25mA	64.0%
450°C	50mT	0.843V	1.36mA	64.0%
400°C	25mT	0.818V	1.25mA	62.1%
425°C	25mT	0.819V	1.30mA	62.0%
450°C	25mT	0.810V	1.33mA	62.8%
Standard	100mT	0.918V	1.10mA	64.7%

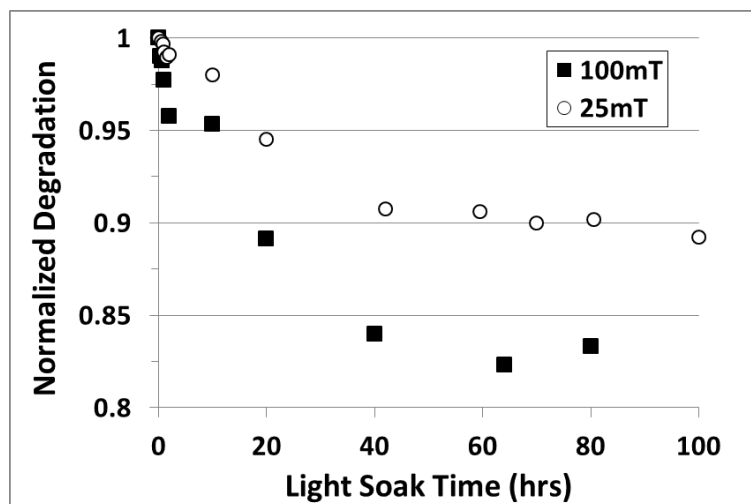
QE measurements in Figure 5-10 indicate that the 25mT sample shifts further toward the red wavelengths as the band gap decreases. The QE ratio results are promising though. For all wavelengths, the 25mT sample stays at or below a ratio of 1.2 while the 100mT sample has a slight hole collection problem as indicated by the 1.4 ratio at 800nm.

**Figure 5-10. QE and QE ratio for high temperature devices fabricated at two different pressures.**

## CHAPTER 6 - STABILITY RESULTS FOR HIGH TEMPERATURE, LOW PRESSURE DEVICES

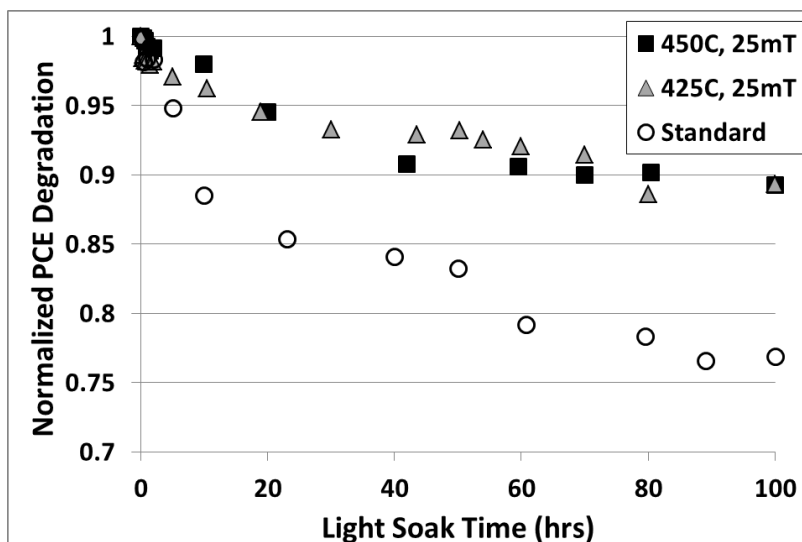
### 6.1 High Temperature Device Degradation

Characterization of the high temperature, low pressure devices showed good properties like low defects and good hole collection in the QE ratio (see 6.2-6.4). Light soaking was performed to see if it improved degradation. The results are given in Figure 6-1 and 6-2. In Figure 6-1, two devices fabricated at 450°C are compared. The device fabricated with a chamber pressure of 25mT degraded by only 10% while the 100mT device dropped by over 15%. This figure shows that fabrication pressure plays an impact in material composition and improves degradation when ion bombardment is increased.



**Figure 6-1. Results of light soaking compared to a 100mT device.**

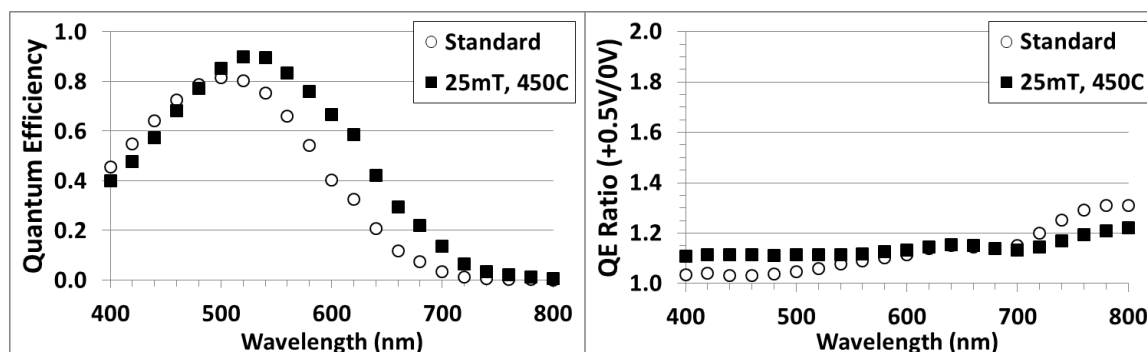
Figure 6-2 compares two high temperature samples, both deposited at 25mT, to the standard sample. As shown previously, the standard sample degrades by almost 25%, but both high temperature samples degrade by only 10%. It seems from this result that temperature plays less of a role than pressure which might be predicted based on our previous results with high temperature at 100mT where degradation only improved slightly.



**Figure 6-2. Comparison of degradation of low pressure devices to standard sample. Degradation of efficiency is only 10% for both devices whereas degradation is almost 25% for the standard sample.**

## 6.2 Quantum Efficiency

Comparing the QE of these samples to the standard confirms the larger current densities measured with I-V. The QE ratio in Figure 6-3 also shows that the experimental devices have better hole collection even up to 800nm. After degradation these curves just decline uniformly across all wavelengths. QE ratios for the low pressure device only increase to 1.25 at 800nm after degradation, indicating strong hole collection even after exposure to light. This data backs up the degradation data shown in Figure 6-2.

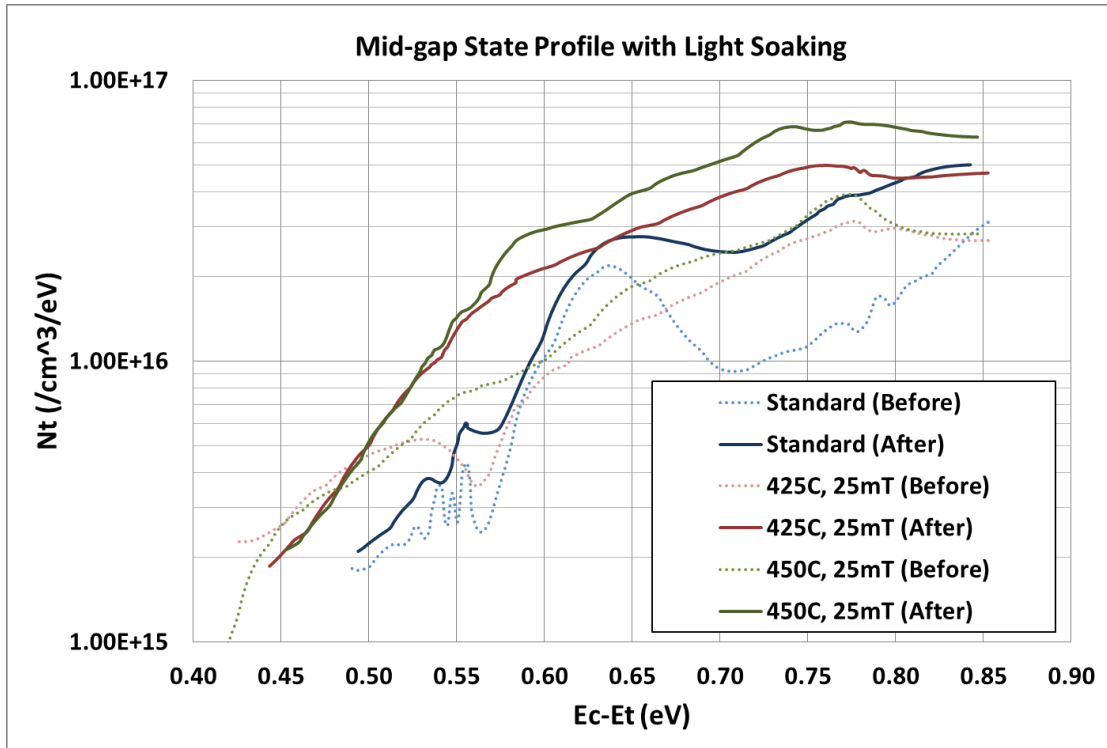


**Figure 6-3. QE and QE ratio for high temperature, low pressure device compared to standard.**

### 6.3 Defect Density Changes

As discussed in Chapter 1 and throughout this study, light soaking has been shown to create midgap defect states that increase recombination and reduce the built-in electric field. Thus, it is desired to know how defects are changing in these devices which degrade less by using capacitance measurements as outlined in Chapter 3.

From capacitance versus frequency measurements the defect profile is found before and after light exposure. Figure 6-4 shows the result with dotted lines indicating before light exposure and solid lines being after. Oddly, the defect profile shows higher densities for the samples which degraded less. That change from before to after is similar for all samples. It is interesting to see how the profile changes for a given sample though. Defects at midgap seem to approximately double while at lower energies there is less increase showing that degradation does indeed seem to be a result of midgap defects being generated.



**Figure 6-4. Comparison of defect profile for three samples before and after degradation found using C-f.**

**Table 6-1. Defect densities before and after light soaking as measured by C-V at 20Hz and 150°C.**

Growth Temperature	Growth Pressure	Defect Density Before (cm <sup>-3</sup> )	Defect Density After (cm <sup>-3</sup> )
Standard 300°C	100mT	2.07E+16	1.10E+17
425°C	25mT	2.47E+16	2.71E+16
450°C	25mT	2.47E+16	2.80E+16

Another method of measuring defects over all energies throughout the intrinsic layer is with capacitance versus voltage using 150°C at 20Hz (or lower) as described in Chapter 3. The measured values from before and after light soaking are given in Table 6-1. These results match what would be expected based on Figure 6-2. The measurements show that defects increase greatly for the standard sample from 2E16 cm<sup>-3</sup> to over 1E17 cm<sup>-3</sup>, almost one order of magnitude larger.

Unlike the standard sample, the two experimental samples fabricated at elevated temperatures in low pressure show only slight changes to their defects. From before to after light exposure, the defects in the sample increase by less than 5E15 cm<sup>-3</sup>. This measurement appears to directly show the cause of the improved stability.

## 6.4 Urbach Energy

Finally, the subgap absorption is studied with the subgap QE measurement (Chapter 3). From these measurements, the exponential valence tail states are quantified based on their Urbach energies. Table 6-2 gives the result of these measurements for the same three devices as in the previous sections.

From the subgap QE measurements, little can be obtained other than the trends which appear. After light soaking, samples seem to degrade a little or stay the same in relation to Urbach energy (within the error of measurement). This indicates that either the valence tail states are not changing at all or not drastically enough to see in this measurement. There is no correlation to the degradation results as far as this data shows.

**Table 6-2. Urbach energies measured before and after light soaking as measured with subgap QE.**

Growth Temperature	Growth Pressure	Urbach Energy Before (meV)	Urbach Energy After (meV)
Standard 300°C	100mT	43.5	45.6
425°C	25mT	52.2	51.8
450°C	25mT	53.0	56.8

As expected, the high temperature samples have a much larger Urbach energy due to the “worse” film quality created under these conditions. These devices don’t seem to degrade based on the valence tail states. Based on the measurements conducted and presented, the cause of device degradation appears to be the creation of midgap defects which can be detected by capacitance measurements at low frequency and high temperature.



## CHAPTER 7 - CONCLUSION

This study attempted to find a technique for fabrication of hydrogenated amorphous silicon solar cells via PECVD which reduced light-induced degradation without causing a decline in the time it takes to make each device. After systematically trying different solutions based primarily on thermal and chemical annealing, a process was discovered that improves a-Si:H solar cell stability.

The method of reducing light-induced degradation uses elevated fabrication temperature with lower chamber pressures when depositing the all-important intrinsic layer. This is supplemented with the use of (ppm) boron grading to augment the built-in electric field, aiding collection of photo-generated charge carriers. The increased ion energy from lower chamber pressure plus the added thermal energy of using high temperatures produces devices with initial efficiencies over 6%. After degradation, the change in the number of midgap defects is much less in these devices, resulting in less degradation compared to standard devices. After 100 hours of exposure to AM1.5 light at twice sun intensity, the sample fabricated at 450°C and 25mT degraded by only 10%. By comparison, the standard device degraded by almost 25% under the same conditions.

The presented process of creating a-Si:H solar cells is done during fabrication and does not require extra time to complete besides the time for heating and cooling. Thus, this fabrication technique could be transitioned easily to commercial production with very little adjustments. With further research, this method could be perfected to create a-Si:H solar cells which degrade minimally while still providing manageable efficiencies on flexible substrates with a plethora of applications.

## APPENDIX - IMPROVING THE STABILITY OF AMORPHOUS SILICON SOLAR CELLS

A paper submitted to the *Journal of Applied Physics*

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### Abstract

A new technique for improving the stability of amorphous silicon p-i-n solar cells is introduced. The technique consists of deposition at higher temperatures than normal, ~400-425 °C, and at lower pressures, so that significant ion bombardment can occur during growth. In addition, ppm levels of B grading is introduced in the intrinsic layers of the device so as to provide a built-in field to assist in hole collection and thereby achieve good performance for the cell. The combination of these techniques leads to a reduction in degradation of the cell to ~10% as opposed to over 20% for a standard cell. Measurements of quantum efficiency, subgap quantum efficiency, and defect density using capacitance spectroscopy confirm that the new cell material is much more stable than standard p-i-n cells with identical thickness of the intrinsic layer.

### I. Introduction

Ever since the discovery of the Staebler-Wronski effect [1], the stability of amorphous silicon (a-Si:H) solar cells upon light soaking has been a major problem. Various methods have been used to reduce such degradation in a-Si:H solar cells, including the use of chemical annealing [2] and the use of slow growth techniques [3]. The degradation in the

output of the cell is due to an increase in mid-gap defect density in the intrinsic layer of the cell upon light soaking [4], which then causes a decrease in the carrier mobility-lifetime ( $\mu\tau$ ) product and also a decrease in the electric field in the middle of the cell [5]. The combination of a lower  $\mu\tau$  product and a decrease in electric field (F) in the middle of the intrinsic layer leads to a decrease in the range,  $\mu\tau F$ , particularly under the operating condition of the cell where it is operating under a forward bias and therefore, at a lower field. This in turn leads to a precipitous decrease in the fill factor of the cell [5,6]. The reason for the increase in the midgap density appears to be the presence of weak Si-H bonds, e.g. in clustered Si-H bonds which may be present on the internal surfaces of voids in the material [7-9].

From the above discussion, it is clear that to improve the stability of the cell, one needs to reduce the number of clustered Si-H bonds, and also simultaneously improve the electric field in the middle of the intrinsic layer of the cell. Recently, Bobela et al [10] showed that it may be possible to reduce the growth in defect density in the material upon light soaking by doing a high temperature, post-growth anneal on the a-Si:H material. In this paper, we examine the impact of such anneal on the stability of solar cells, and show that it leads to a high defect density and does not lead to better stability of the cell. We then show that a new technique, which combines higher temperature growth, with a lower pressure deposition, combined with a ppm level doping of boron in the middle of the intrinsic layer leads to both less defect generation, better hole collection and significantly better stability for devices.

## **II. Experimental Techniques**

The experiments were done using a plasma-CVD reactor for depositing the p, i and n layers of the device. The devices were deposited on polished stainless steel substrates. The

frequency was  $\sim 45$  MHz. The pressure was 100mT. The hydrogen/silane ratio for the growth of the intrinsic layer was  $\sim 20:1$ . For post-anneal experiments similar to the work by Bobela et al [10], the growth of the device, which was deposited at  $\sim 250$  °C, was interrupted after the n and i layers, and the samples were annealed in a hydrogen atmosphere at  $\sim 450$  °C. The p layer was deposited after the anneal, since high temperature annealing of the completed p-i-n device always led to significant B diffusion into the i layer, thereby ruining the device. A final ITO layer completed the cell. Some devices were provided with an additional built-in field in the i layer by using graded ppm levels of B doping, with B level increasing as the thickness of the i layer increased. See Fig. 1 for a schematic band diagram of the i layer of the device with the graded B doping.

For devices deposited using our new technique, the device run was continuous. The devices were deposited at varying temperatures from 250 °C to 425 °C. The devices always had built-in ppm levels of B grading with increasing B content in the middle two third of the device as the thickness of the i layer increased. This was done so as to provide a built-in electric field in the middle of the device.

The devices were measured for their illuminated I-V curves, quantum efficiency under zero bias and under forward bias [11], subgap QE to deduce Urbach energy and midgap defect density [12], and C-V measurements done at 150 °C and 20 Hz so as to deduce the total defect density.

### **III. Results on Post-deposition Annealed Cells**

In Fig. 2, we show the I-V curve for a cell which was subjected to post-deposition anneal at a higher temperature of 450 °C and for comparison, also an I-V curve for a cell prepared under normal conditions and not subjected to an anneal. The I-V curve of the high

temperature annealed cell is rather poor, with a poor fill factor (58%) indicating poor hole collection. The quantum efficiency (QE) curve, and the QE ratio curves for this cell are shown in Fig. 3 and compared with the QE and QE ratio curves for a cell prepared without thermal annealing. The QE ratio is the ratio of QE at 0 V to QE under forward bias of 0.5V. The QE ratio at longer wavelengths (where the absorption coefficient is low and holes are generated throughout the material), is a sensitive measure of the  $\mu\tau$  product of the material, since under forward bias, the electric field, and hence the range, decreases. If the range becomes comparable to the thickness because  $\mu\tau$  product is low, then the hole collection suffers, and one gets a reduction in QE under forward bias, resulting in a higher ratio [13]. The data of Fig. 3 shows that for the higher temperature device, the QE ratio is rather high at longer wavelengths, implying poor hole collection compared to a cell prepared at a temperature of 250 °C and not annealed.

The device performance and QE ratio of the cell which was thermally annealed can be improved by using graded B doping, as shown in Fig.4 for the I-V curve and Fig. 5 for QE and QE ratio. The fill factor increased to 62%, and the QE ratio at 800nm decreased to 1.2 from 1.4 in Fig. 3, both factors clearly indicating that graded doping of the intrinsic layer was helping in hole collection.

The improved sample was then subjected to light illumination for 100 hours at 2x sun intensity from a full solar spectrum xenon solar simulator. For comparison, a standard device sample with a good fill factor (64.7%) fabricated at 250 °C was also subjected to the same illumination. Both devices had the same thickness of the intrinsic layer, about 0.3 micrometer, in a p-i-n configuration. The results of the degradation test are shown in Fig. 6 for both these samples. The corresponding changes in QE ratio are shown in Fig. 7. The QE

ratio at longer wavelengths increases significantly for both types of samples after degradation. From the figure, it is apparent that the high temperature annealed device degrades almost the same amount as the standard device. This result contradicts the earlier results from Bobela et al on stability of materials [10]. Perhaps, the discrepancy is due to the fact that Bobela et al [10] measured only the defect density in a film which could be affected by surface conditions, whereas we are measuring collection properties in a device which are not affected by surfaces.

#### **IV. Results on Samples Prepared at Higher Temperatures**

In Fig. 8, we show the illuminated I-V data on samples which were prepared using a high temperature growth (without post-deposition anneal) at two different pressures (100 mTorr and 25 mTorr). Both samples had ppm levels of B grading, since we have shown earlier that such grading helps in improving device performance, particularly for samples prepared at higher temperature. The objective of changing the pressure was to see if a lower pressure, which increases both ion flux and ion energy impinging on the substrate [14] has an impact on the electronic properties and stability. Fig. 8(a) shows the I-V curve for a device prepared at 100 mTorr and 400 °C and 8(b), for the sample prepared at 25 mTorr. Both curves have been compared to the data for a standard cell deposited at 250 °C and 100 mTorr pressure. The sample prepared at higher temperature has a lower  $V_{oc}$  and higher current than the sample prepared at lower temperatures, a consequence of its smaller bandgap. The fill factors are quite reasonable for both sets of samples. The figures show that deposition at a lower pressure reduces open-circuit voltage compared to deposition at the same temperature but at 100 mTorr pressure. This fact indicates that increasing ion bombardment is affecting the bandgap and perhaps H bonding [15]. Fig. 9, which shows the QE and QE ratios for the

two samples confirm that the quality of the two samples is very similar, except that the sample prepared at higher temperature has a QE that is higher in the infrared region of the spectrum compared to the sample prepared at a lower temperature, a consequence of its smaller bandgap.

Next, we subjected these samples to AM1.5 illumination from a full spectrum xenon solar simulator from ABET under 2x sun ( $200\text{mW}/\text{cm}^2$ ) intensity. First, we show the comparison of changes in efficiency vs. time for the two samples, one prepared at 100 mTorr and the other, at 25 mTorr. It is apparent from Fig. 10 that the sample prepared at 25 mTorr is more stable than one prepared at 100 mTorr. We next compare the stability of the sample prepared under low pressure, high temperature conditions with the stability of a standard cell prepared at 250 °C. See Fig. 11. It is apparent from Fig. 11 that a combination of higher temperature growth and lower pressure does lead to a more stable sample. The QE ratio data for the standard sample, and the higher temperature, lower pressure sample, taken after degradation also confirm that indeed, the higher temperature grown sample has less loss in hole collection after degradation than the standard sample.

## **V. Data on Subgap Absorption and Defect Densities**

In Fig. 12, we show the subgap absorption data on a standard sample, and on the sample prepared at 400 °C with 25 mTorr deposition. Both samples have reasonable Urbach energies, in the range of ~45 meV. The subgap QE curve is shifted to lower energies compared to the subgap QE for the standard cell, a consequence of both the higher growth temperature and higher ion bombardment. The midgap defect density appears to be in the same range as the standard sample.

We also measured the total defect densities in these devices by using a low frequency, high temperature C-V measurements. At 20 Hz and 150 °C, assuming an attempt to escape frequency of  $10^{12}/s$ , this technique allows a probing of all the defects from the conduction band down to  $\sim 0.85$  eV below the conduction band. The defect density in the standard device was  $2.1 \times 10^{16}/cm^3$  and in our higher temperature, lower pressure device was  $2.5 \times 10^{16}/cm^3$ . We also measured the defect density after degradation, and found that indeed, the defect density was much more in the standard sample after degradation when compared to the sample prepared at higher temperature and lower pressure ( $1.1 \times 10^{17}/cm^3$  vs.  $2.8 \times 10^{16}/cm^3$ ).

## **VI. Conclusion**

In conclusion, we have shown that the strategy of post-deposition anneal to improve stability does not seem to help in improving the stability of devices. In contrast, we have developed a new technique which relies on controlled ion bombardment, higher temperature growth and ppm levels of B grading to improve the localized field, which improves the stability of devices while keeping good device properties.

This work was partially supported by a NSF grant and was carried out at the Microelectronics Research Center of Iowa State University.



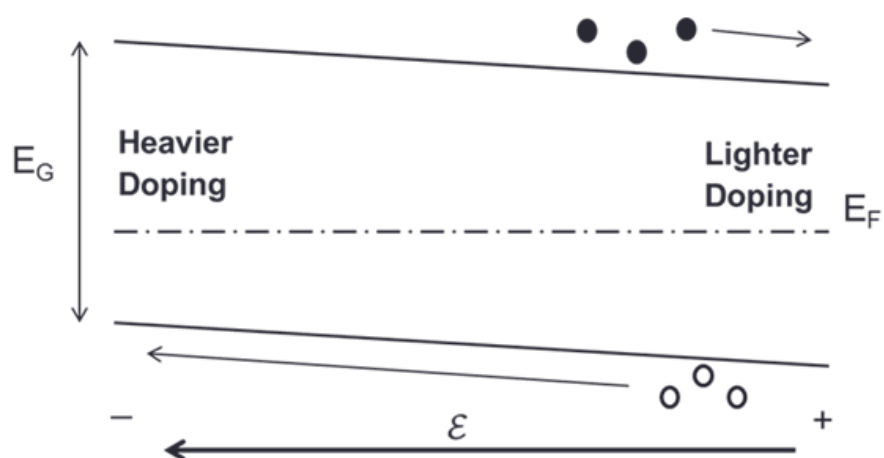


Figure 1. Energy band diagram for the intrinsic layer in a p-i-n cell when doped with ppm levels of B with B concentration increasing from the n layer to the p layer.

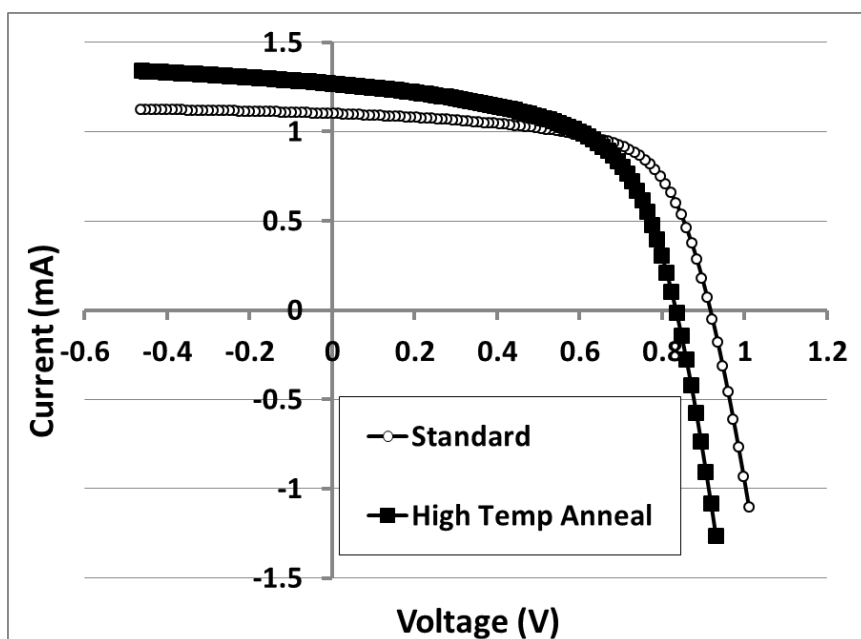


Figure 2. Illuminated I-V curve for two solar cells, one prepared using standard conditions at 250 °C, and the other subjected to post-deposition anneal at 425 °C.

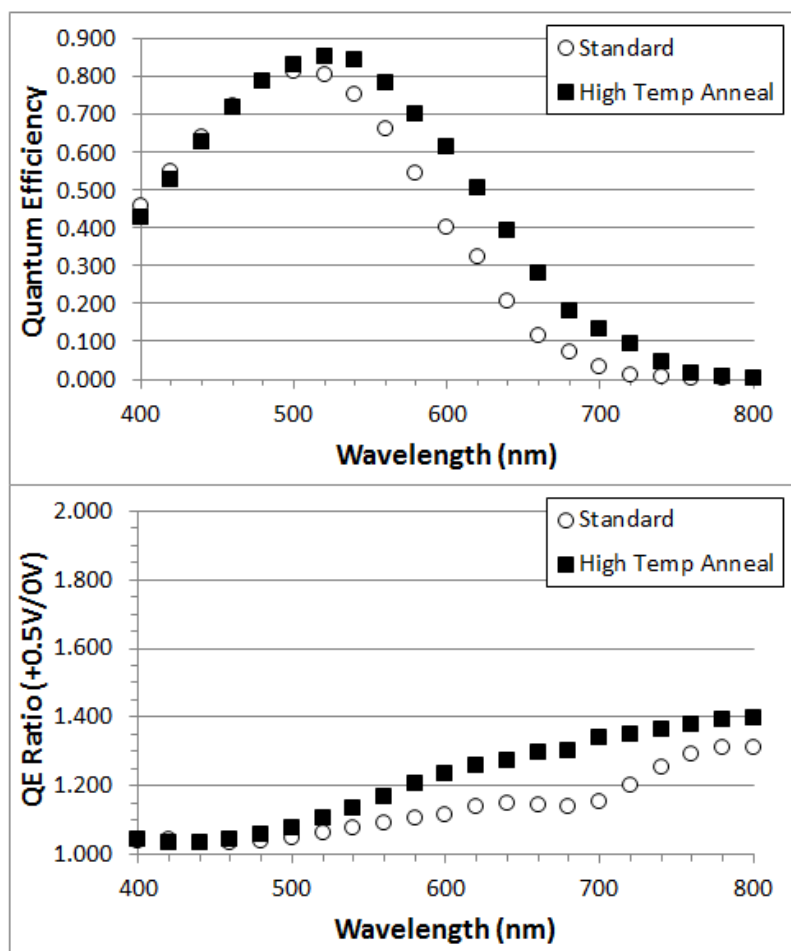


Figure 3. Quantum efficiency (QE) and QE ratio [QE at 0V/QE at +0.5V] vs. wavelength for the standard cell and the post-deposition annealed cell. A higher ratio in the infrared region indicates that holes require a higher electric field than is present under forward bias in order to be collected, i.e. the mobility-lifetime product of holes is small.

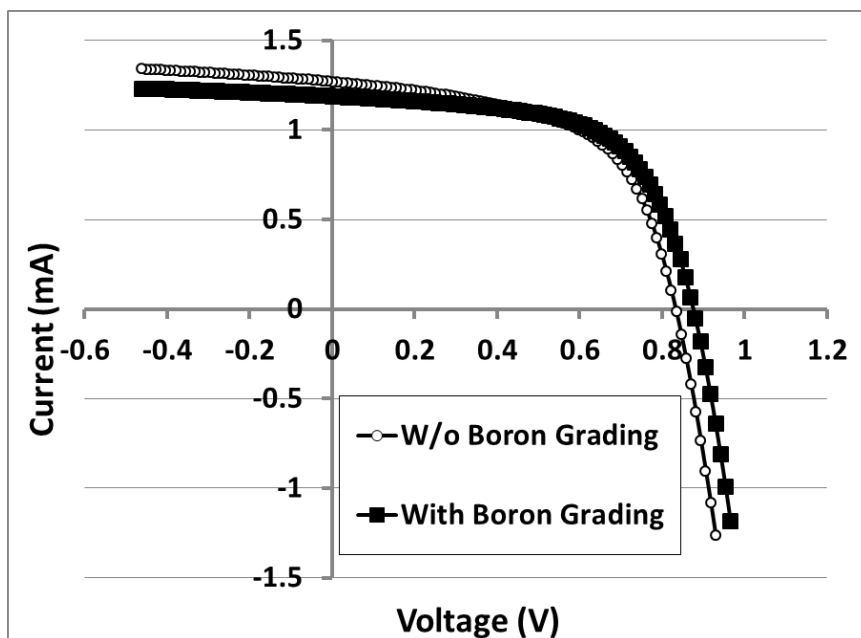


Figure 4. Illuminated I-V curves for two cells prepared using post-deposition anneals, with one cell without ppm levels of B grading in the intrinsic layer, and the other cell with B grading. The cell with B grading has distinctly higher fill factor.

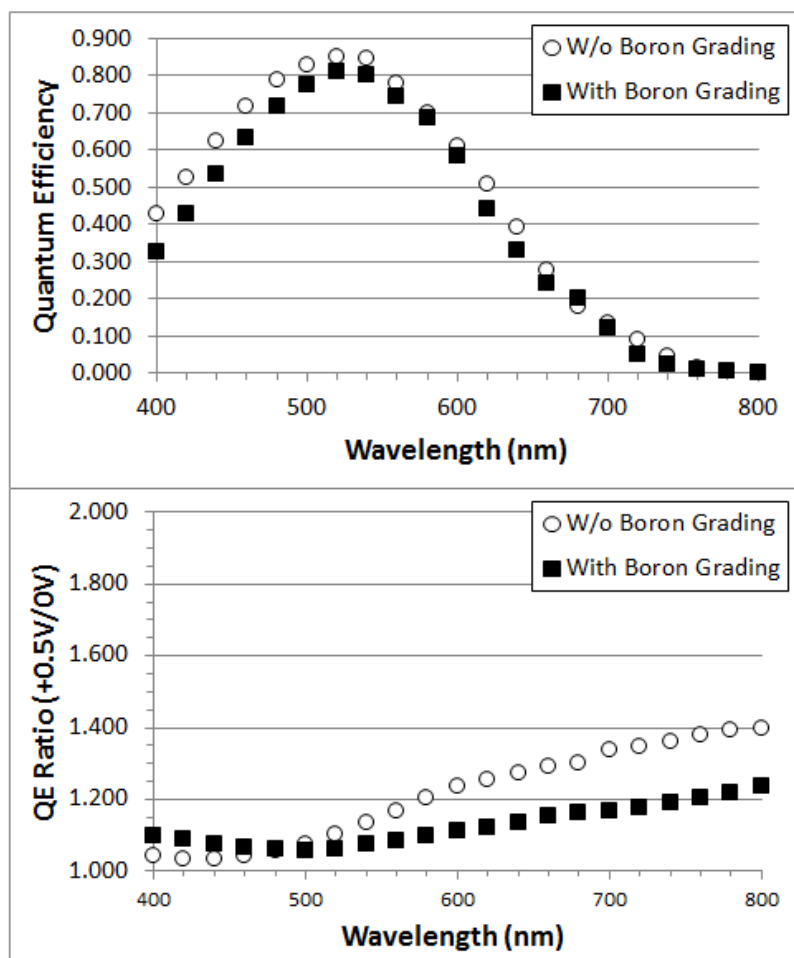


Figure 5. QE and QE ratio curves vs. wavelength for the two cells whose I-V curves were shown in Fig. 5. A lower QE ratio for the B graded cell indicates that the collection of holes is significantly improved by having a built-in field.

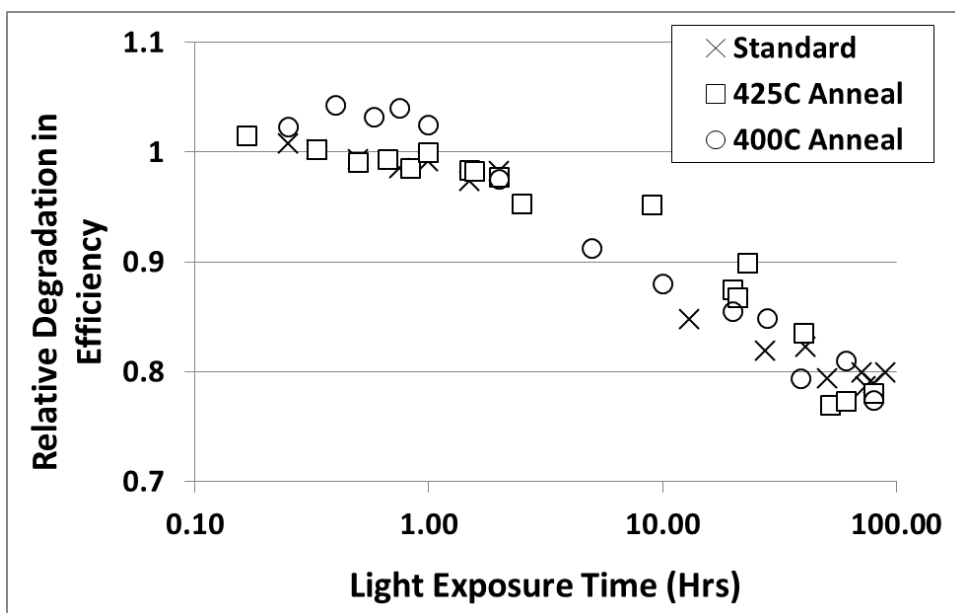


Figure 6. Data on changes in efficiency of solar cells over time when subjected to 2X sun illumination. There does not appear to be any improvement in stability when the intrinsic layers of solar cells are subjected to post-deposition anneals.

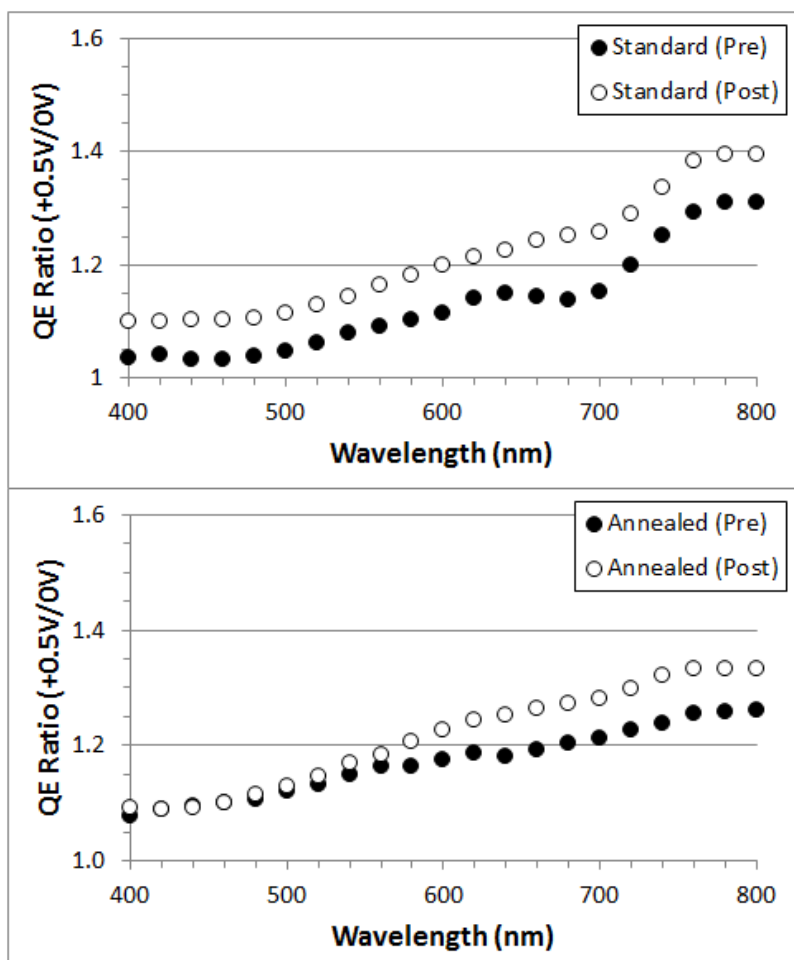


Figure 7. Data on QE ratio curves vs. wavelength for standard cell (top) and annealed cell (bottom) before and after degradation. The QE ratio curves are for both cells after degradation are very similar, indicating similar degradation, in agreement with the data shown in Fig. 6.

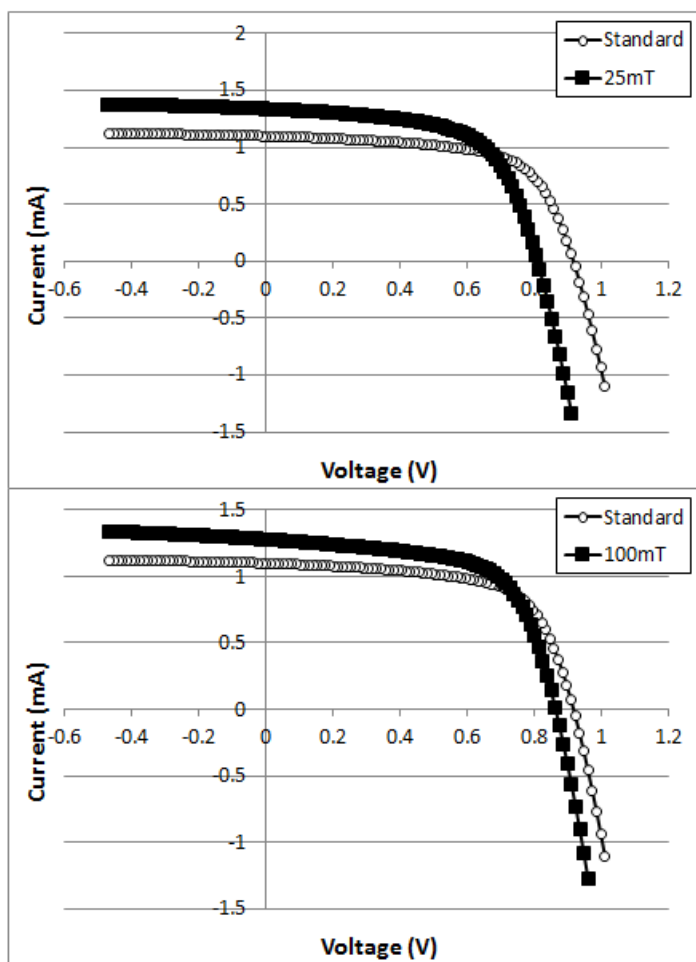


Figure 8. I-V curves for two sets of cells prepared at higher temperatures with B grading. The top panel shows the comparison I-V curves for a cell prepared at 25 mTorr pressure and ~425 °C and a standard cell prepared at 250 °C, and the bottom panel shows a comparison between the standard cell and a cell prepared at 100 mTorr pressure and 425 °C. The lower voltages and higher currents for cells prepared at higher temperatures are a consequence of the shrinking of the bandgap with temperature. Note that the fill factor for the cell prepared at 25 mTorr is similar (~63%) to the fill factor for the cell prepared at higher pressure (64%).

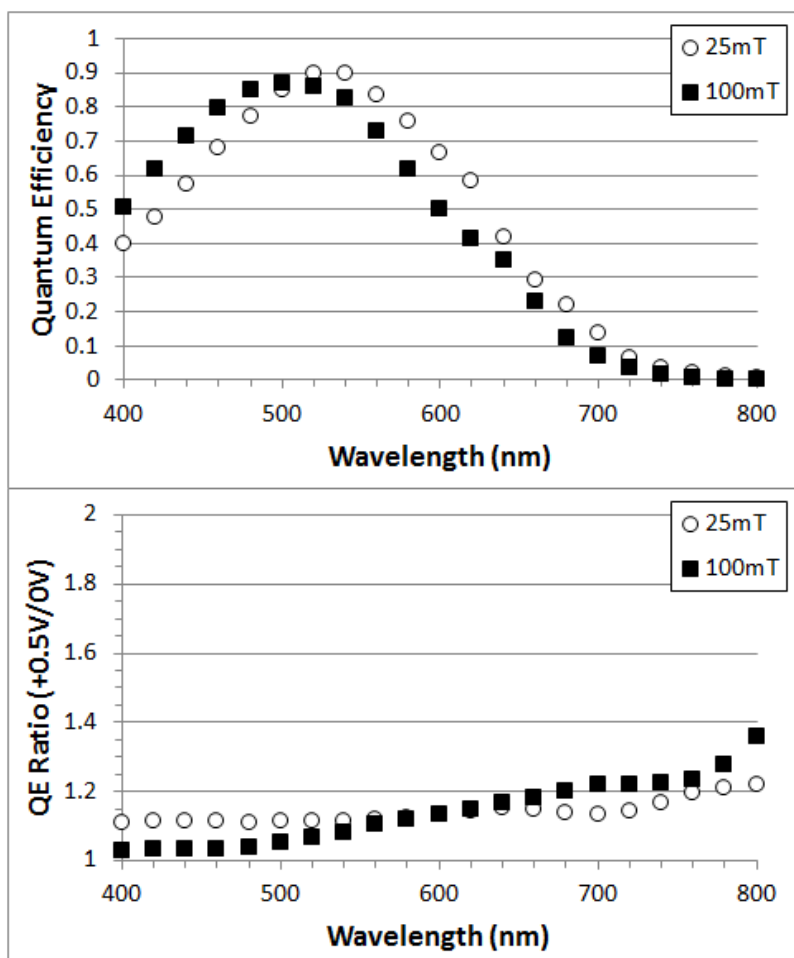


Figure 9. QE and QE ratio curves for the two cells prepared at higher temperature with B grading. The QE ratio in the infrared for the cell prepared at 100 mTorr is higher than one for the cell prepared at 25 mT indicating a poorer collection of holes in the 100mTorr cell.



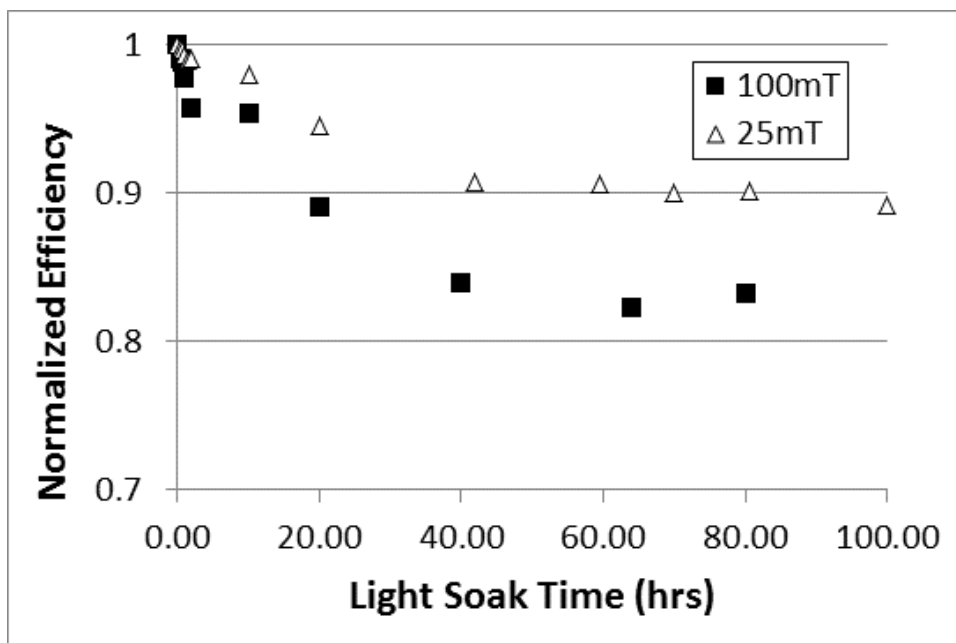


Figure 10. Comparison of the decrease in efficiency vs. time upon light soaking under 2X sun for the cells prepared at 25 mTorr and 100 mTorr. The results indicate that the cell prepared at 25 mTorr degrades much less than the one prepared at 100 mTorr.

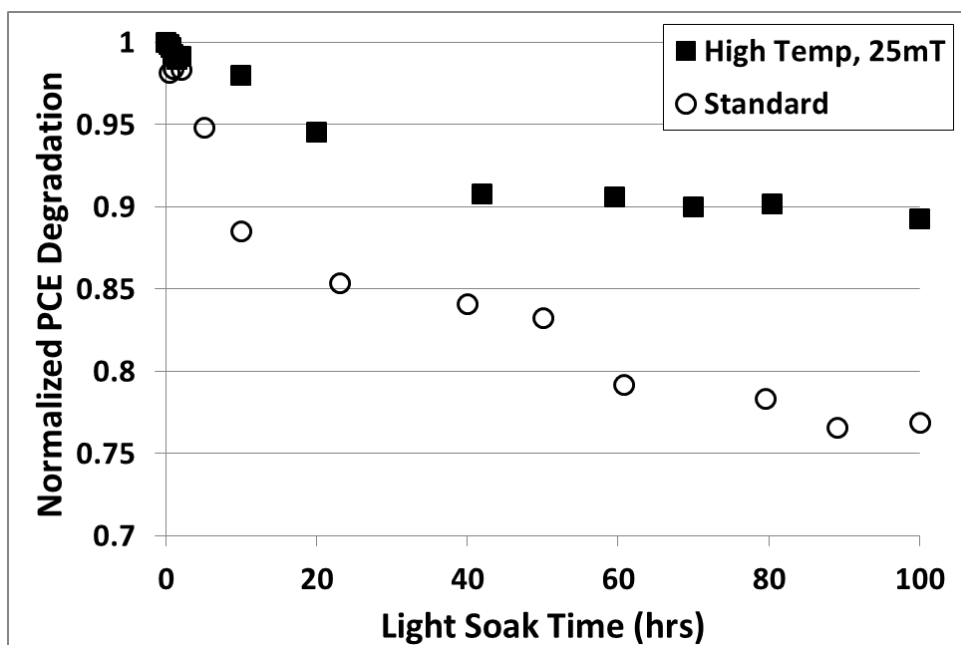


Figure 11. Comparison of changes in efficiency vs. time under 2X sun illumination for the 25 mTorr cell and the standard cell, showing a significantly better stability for the cell prepared at higher temperature, lower pressure and ppm levels of B grading.

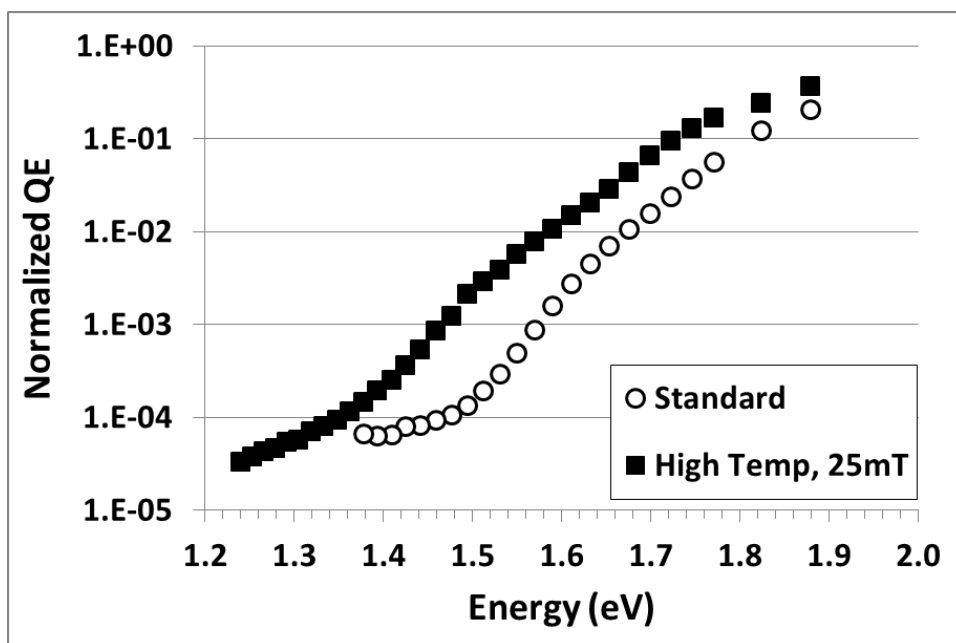


Figure 12. Subgap QE vs. wavelength curves for the standard cell and the 25 mTorr, higher temperature cell, showing approximately equal Urbach energies, but a shift in the curve to lower energies for the higher temperature cell, indicating a lower bandgap.

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